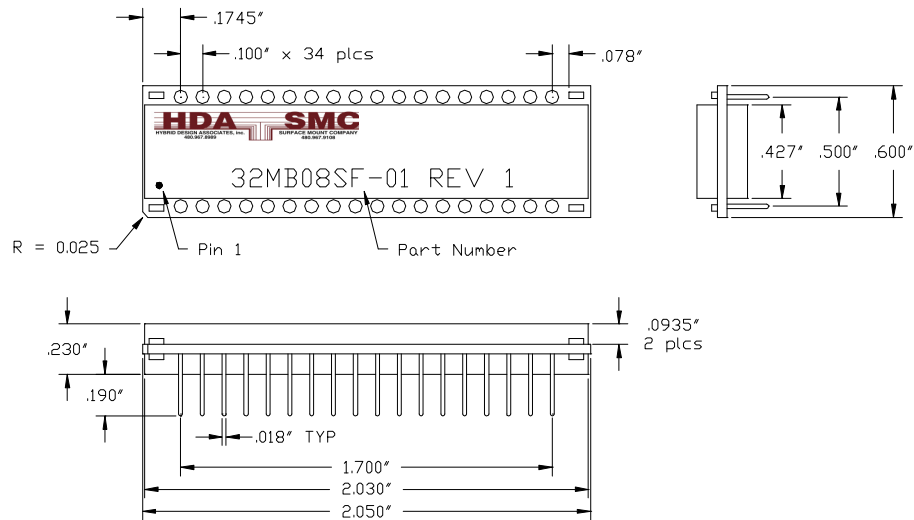


HIGH TEMPERATURE 32MB SPI SERIAL FLASH MEMORY MODULE

PART NUMBER 32MB08SF-01

CMOS 3.0 Volt-only 8-bit



Characteristics

- 2.7 – 3.6 VOLT FOR READ AND PROGRAM OPERATIONS
- SPI BUS COMPATIBLE SERIAL INTERFACE
- SECTOR ERASE ARCHITECTURE
- SUPPORTS FULL CHIP ERASE
- EMBEDDED ERASE ALGORITHMS
- EMBEDDED PROGRAM ALGORITHMS
- PROGRAM CYCLES ON A PAGE BY PAGE BASIS (256 BYTES IN A PAGE)
- 50 MHZ CLOCK RATE SUPPORTS 10 MEGABITS PER SECOND READ RATE (MAXIMUM)
- WRITE PROTECT PIN WORKS WITH STATUS REGISTER TO PROTECT PORTIONS OF MEMORY
- LOW POWER CONSUMPTION
- POWER SAVING STANDBY MODE
- HOLD PIN PAUSES SERIAL COMMUNICATION WITHOUT DESELECTING DEVICE
- DESIGNED FOR HIGH TEMPERATURE APPLICATIONS

PIN DESCRIPTION

1	NC	36	VCC (3.0 VOLTS)
2	A_H0	35	VCC (3.0 VOLTS)
3	NC	34	#WP
4	A_H1	33	GND
5	NC	32	#HOLD
6	A_H2	31	GND
7	NC	30	CLK
8	A_H3	29	GND
9	NC	28	DATA_IN
10	A_H4	27	GND
11	NC	26	DATA_OUT
12	NC	25	GND
13	CE_L	24	NC
14	NC	23	GND
15	GND	22	NC
16	GND	21	GND
17	NC	20	NC
18	NC	19	NC

Table 1 Signal Description

VCC	Power Supply - + 3 V DC
A_H[4..0]	Address Bus
#HOLD	Hold Input – Active Low
#WP	Write Protect Input – Active Low
CLK	Serial Clock Input
DATA_IN	Serial Data Input
DATA_OUT	Serial Data Output
GND	Ground

GENERAL DESCRIPTION

HDA-SMC reserves the right to change or discontinue work on this product without notice.

The Flash Memory Module 32MB08SF contains 32 Serial Flash Memory ICs. The address bus pins are provided to activate individual chip enable inputs on each IC.. Each flash memory device can be read in a random access manner. Writes, however, are done on a byte-by-byte basis and strict write procedures need to be followed. Before writing to a location in memory, that memory must first be erased. This can be done on a sector basis, or it can be done on a chip wide basis. It is possible to program the individual memory chips to enter erase cycles at the same time. Care should be taken that the thermal limits of the device are not exceeded and that the power supply can provide the necessary current. It is recommended that the chips be individually erased. It is also possible to have more than one chip in a write mode at the same time. Care should be taken when causing more than one chip to be in the write state.

Signal Description

Signal Data Output (SO):

This output signal is used to transfer data serially out of the device. Data is shifted out on the falling edge of Serial Clock (SCK).

A_H[4..0]

Address bus used to address one of 32 devices within the 32MB08SF module.

Serial Data Input (SI):

This input signal is used to transfer data serially into the device. It receives instructions, addresses, and the data to be programmed. Values are latched on the rising edge of Serial Clock (SCK).

Serial Clock (SCK):

This input signal provides the timing of the serial interface. Instructions, addresses, and data present at the Serial Data input (SI) are latched on the rising edge of Serial Clock (SCK). Data on Serial Data Output (SO) changes after the falling edge of Serial Clock (SCK).

Chip Enable (CE_L):

When this input signal is High, the devices are deselected and Serial Data Output (SO) is at high impedance. Unless an internal Program, Erase or Write Status Register cycle is in progress, the devices will be in Standby mode. Driving Chip Enable (CE_L) Low enables the devices, placing them in the active power mode.

After Power-up, a falling edge on Chip Enable (CE_L) is required prior to the start of any instruction.

Hold (HOLD#):

The Hold (HOLD#) signal is used to pause any serial communications with the device without deselecting the device. During the Hold instruction, the Serial Data Output (SO) is high impedance, and Serial Data Input (SI) and Serial Clock (SCK) are Don't Care.

To start the Hold condition, the device must be selected, with Chip Enable (CE_L) driven Low.

Write Protect (WP#):

The main purposes of this input signal are to freeze the size of the area of memory that is protected against program or erase instructions (as specified by the values in the BP1 and BP0 bits of the Status Register).

SPI Modes

These devices can be driven by a microcontroller with its SPI peripheral running in either of the two following modes:

- CPOL = 0, CPHA = 0
- CPOL = 1, CPHA = 1

For these two modes, input data is latched in on the rising edge of Serial Clock (SCK), and output data is available from the falling edge of serial clock (SCK).

The difference between the two modes, as shown in Figure 2, is the clock polarity when the bus master is in Standby and not transferring data:

- SCK remains at 0 for (CPOL = 0, CPHA = 0 Mode 0)
- SCK remains at 1 for (CPOL = 1, CPHA = 1 Mode 3)

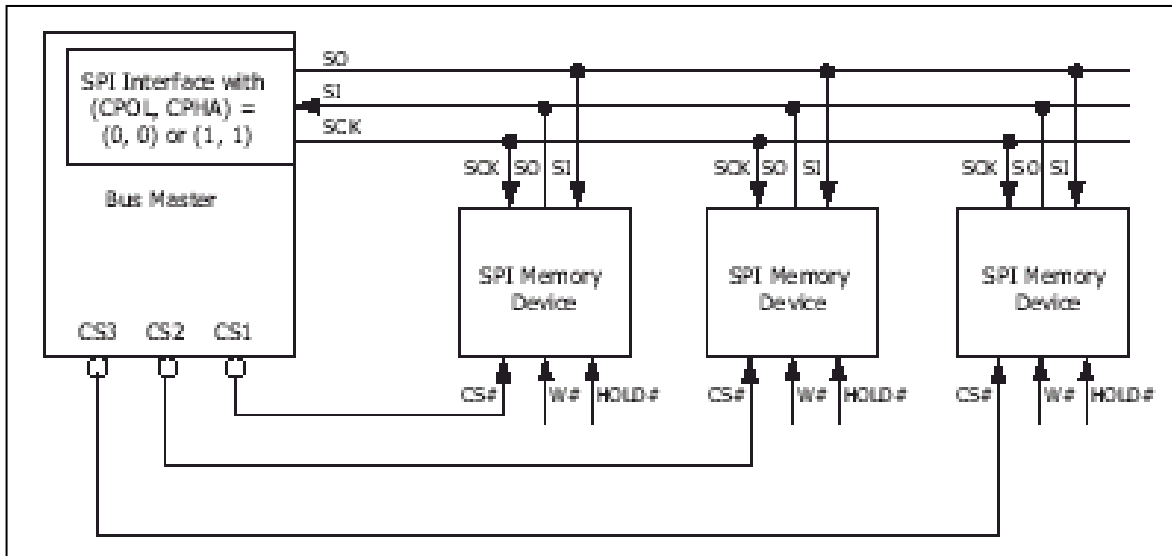


Figure 1 Bus Master and Memory Devices on the SPI Bus

Note: The Write Protect and Hold signals should be driven, High or Low as appropriate.

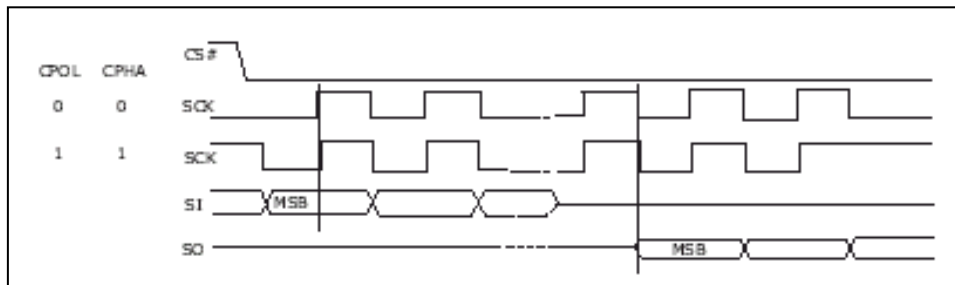


Figure 2 SPI Modes Supported

Operating Features

All data into and out of the device is shifted in 8-bit chunks.

Page Programming

To program one data byte, two instructions are required: Write Enable (WREN), which is one byte, and a Page Program (PP) sequence, which consists of four bytes plus data. This is followed by the internal Program cycle. To spread this overhead, the Page Program (PP) instruction allows up to 256 bytes to be programmed at a time (changing bits from 1 to 0), provided that they lie in consecutive addresses on the same page of memory.

Sector Erase, or Bulk Erase

The Page Program (PP) instruction allows bits to be programmed from 1 to 0. Before this can be applied, the bytes of the memory need to be first erased to all 1's (FFh) before any programming. This can be achieved in two ways: 1) a sector at a time using the Sector Erase (SE) instruction, or 2) throughout the entire memory, using the Bulk Erase (BE) instruction.

Polling During a Write, Program, or Erase Cycle

A further improvement in the time to Write Status Register (WRSR), Program (PP) or Erase (SE or BE) can be achieved by not waiting for the worst-case delay. The Write in Progress (WIP) bit is provided in the Status Register so that the application program can monitor its value, polling it to establish when the previous Write cycle, Program cycle, or Erase cycle is complete.

Active Power and Standby Power Modes

When Chip Enable (CE_L) is Low, the device is enabled, and in the Active Power mode. When Chip Enable (CE_L) is High, the device is disabled, but could remain in the Active Power mode until all internal cycles have completed (Program, Erase, and Write Status Register). The device then goes into the Standby Power mode. The device consumption drops to ISB. This can be used as an extra Deep Power Down on mechanism, when the device is not in active use, to protect the device from inadvertent Write, Program, or Erase instructions.

Status Register

The Status Register contains a number of status and control bits, as shown in [Figure 7](#), that can be read or set (as appropriate) by specific Instructions

WIP bit: The Write In Progress (WIP) bit indicates whether the memory is busy with a Write Status Register, Program or Erase cycle.

WEL bit: The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch.

BP2, BP1, and BP0 bits: The Block Protect (BP2, BP1, and BP0) bits are non-volatile. They define the size of the area to be software protected against Program and Erase instructions.

SRWD bit: The Status Register Write Disable (SRWD) bit is operated in conjunction with the Write Protect (W#) signal. The Status Register Write Disable (SRWD) bit and Write Protect (W#) signal allow the device to be put in the Hardware Protected mode. In this mode, the non-volatile bits of the Status Register (SRWD, BP2, BP1, and BP0) become read-only bits.

Data Protection Modes

The module provides the following data protection methods:

The Write Enable (WREN) command: Must be written prior to any command that modifies data. The WREN command sets the Write Enable Latch (WEL) bit. The WEL bit resets (disables writes) on *power-up* or after the device completes the following *commands*:

- Page Program (PP)
- Sector Erase (SE)
- Bulk Erase (BE)
- Write Disable (WRDI)
- Write Status Register (WRSR)

Software Protected Mode (SPM): The Block Protect (BP2, BP1, and BP0) bits define the section of the memory array that can be read but not programmed or erased. [Table 2](#) shows the sizes and address ranges of protected areas that are defined by Status Register bits BP2:BP0.

Hardware Protected Mode (HPM): The Write Protect (W#) input and the Status Register Write Disable (SRWD) bit together provide write protection.

Clock Pulse Count: The device verifies that all program, erase, and Write Status Register commands consist of a clock pulse count that is a multiple of eight before executing them.

Table 2. Protected Area Sizes

Status Register Block Protect Bits			Memory Array				Protected Portion of Total Memory Array
BP2	BP1	BP0	Protected Address Range	Protected Sectors	Unprotected Address Range	Unprotected Sectors	
0	0	0	None	(0)	00000h-FFFFFFh	SA15-SA0	0
0	0	1	F0000h-FFFFFFh	(1)SA15	00000h-EFFFFh	SA14-SA0	1/16
0	1	0	E0000h-FFFFFFh	(2) SA15:SA14	00000h-DFFFFh	SA13-SA0	1/8
0	1	1	C0000h-FFFFFFh	(4) SA15:SA12	00000h-BFFFFh	SA11-SA0	¼
1	0	0	80000h-FFFFFFh	(8) SA15:SA8	00000h-7FFFFh	SA7-SA0	½
1	0	1	00000h-FFFFFFh	(16) SA15:SA0	None	None	All
1	1	0	00000h-FFFFFFh	(16) SA15:SA0	None	None	All
1	1	1	00000h-FFFFFFh	(16) SA15:SA0	None	None	All

Hold Condition Modes

The Hold (HOLD#) signal is used to pause any serial communications with the device without resetting the clocking sequence. Hold (HOLD#) signal gates the clock input to the device. However, taking this signal Low does not terminate any Write Status Register, Program or Erase Cycle that is currently in progress.

To enter the Hold condition, the device must be selected, with Chip Enable (CE_L) Low. The Hold condition starts on the falling edge of the Hold (HOLD#) signal, provided that this coincides with Serial Clock (SCK) being Low (as shown in [Figure 3](#)).

The Hold condition ends on the rising edge of the Hold (HOLD#) signal, provided that this coincides with Serial Clock (SCK) being Low. If the falling edge does not coincide with Serial Clock (SCK) being Low, the Hold condition starts after Serial Clock (SCK) next goes Low. Similarly, if the rising edge does not coincide with Serial Clock (SCK) being Low, the Hold condition ends after Serial Clock (SCK) next goes Low ([Figure 3](#)). During the Hold condition, the Serial Data Output (SO) is high impedance, and Serial Data Input (SI) and Serial Clock (SCK) are Don't Care.

Normally, the device remains selected, with Chip Enable (CE_L) the entire duration of the Hold condition. This ensures that the state of the internal logic remains unchanged from the moment of entering the Hold condition.

If Chip Enable (CE_L) goes High while the device is in the Hold condition, this has the effect of resetting the internal logic of the device. To restart communication with the device, it is necessary to drive Hold (HOLD#) High, and then to drive Chip Enable (CE_L) Low. This prevents the device from going back to the Hold condition.

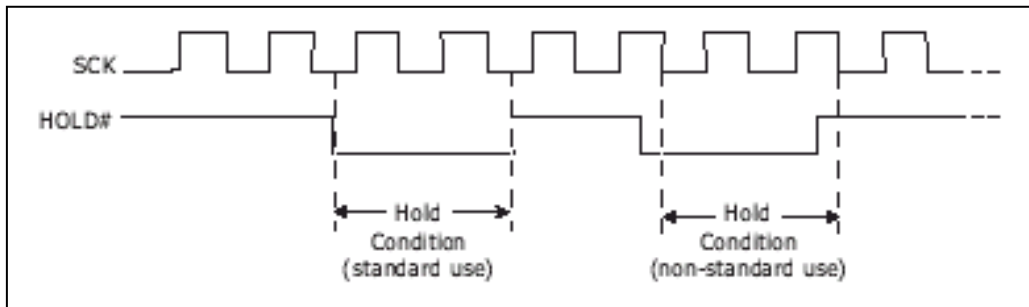


Figure 3 Hold Condition Activation

Memory Organization

The memory is organized as:

- Sixteen sectors of 512 Kbit each
- Each page can be individually programmed (bits are programmed from 1 to 0).
- The device is Sector or Bulk erasable (bits are erased from 0-1).

TABLE 3. Device Organization

Each Device has	Each Sector has	Each Page has	
1,048,576	65,536	256	bytes

TABLE 4. Sector Address Table

Sector	Address Range	
SA15	F0000h	FFFFFh
SA14	E0000h	EFFFFh
SA13	D0000h	DFFFFh
SA12	C0000h	CFFFFh
SA11	B0000h	BFFFFh
SA10	A0000h	AFFFFh
SA9	90000h	9FFFFh
SA8	80000h	8FFFFh
SA7	70000h	7FFFFh
SA6	60000h	6FFFFh
SA5	50000h	5FFFFh
SA4	40000h	4FFFFh
SA3	30000h	3FFFFh
SA2	20000h	2FFFFh
SA1	10000h	1FFFFh
SA0	00000h	0FFFFh

Instructions

All instructions, addresses, and data are shifted in and out of the device, starting with the most significant bit. Serial Data Input (SI) is sampled on the first rising edge of Serial Clock (SCK) after Chip Enable (CE_L) is driven Low. Then, the one byte instruction code must be shifted in to the device, most significant bit first, on Serial Data Input (SI), each bit being latched on the rising edges of Serial Clock (SCK). The instruction set is listed in [Table 5](#).

Every instruction sequence starts with a one-byte instruction code. Depending on the instruction, this might be followed by address bytes, or by data bytes, or by both or none. Chip Enable (CE_L) must be driven High after the last bit of the instruction sequence has been shifted in.

In the case of a Read Data Bytes (READ), Read Status Register (RDSR), Read Data Bytes at higher speed (FAST_READ) the shifted-in instruction sequence is followed by a data-out sequence. Chip Enable (CE_L) can be driven High after any bit of the data-out sequence is being shifted out to terminate the transaction.

In the case of a Page Program (PP), Sector Erase (SE), Bulk Erase (BE), Write Status Register (WRSR), Write Enable (WREN), or Write Disable (WRDI) instruction, Chip Enable (CE_L) must be driven High exactly at a byte boundary, otherwise the instruction is rejected, and is not executed. That is, Chip Enable (CE_L) must be driven High when the number of clock pulses after Chip Enable (CE_L) is driven Low is an exact multiple of eight.

All attempts to access the memory array during a Write Status Register cycle, Program cycle or Erase cycle are ignored, and the internal Write Status Register cycle, Program cycle or Erase cycle continues unaffected

Table 5 Instruction Set

Instruction	Description	One Byte Instruction Code	Address Bytes	Dummy Bytes	Data Bytes
Status Register Operations					
WREN	Write Enable	06H (0000 0110)	0	0	0
WRDI	Write Enable	04H (0000 0100)	0	0	0
RDSR	Read from Status Register	05H (0000 0101)	0	0	1 TO Infinity
WRSR	Write to Status Register	01H (0000 0001)	0	0	1
Read Operations					
READ	Read Data Bytes	03H (0000 0011)	3	0	0
FAST_READ	Read Data Bytes At Higher Speed	0BH (0000 0011)	3	1	1 to infinity
Erase Operations					
SE	Sector Erase	D8H (1101 1000)	3	0	0
BE	Bulk (Chip) Erase	C7H (1100 0111)	0	0	0
Program Operations					
PP	Page Program	02H (0000 0010)	3	0	1 to 256
Deep Power Down Savings Mode Operations					
DP	Deep Power Down	B9H (1011 1001)	0	0	0
RES	Release from Deep Power Down	ABH (1010 1011)	0	0	0
	Release from Deep Power Down and Read Electronic Signature	ABH (1010 1011)	0	3	1 to Infinity

Write Enable (WREN)

The Write Enable (WREN) instruction ([Figure 4](#)) sets the Write Enable Latch (WEL) bit. The Write Enable Latch (WEL) bit must be set prior to every Page Program (PP), Erase (SE or BE) and Write Status Register (WRSR) instruction. The Write Enable (WREN) instruction is entered by driving Chip Enable (CE_L) Low, sending the instruction code, and then driving Chip Enable (CE_L) High.

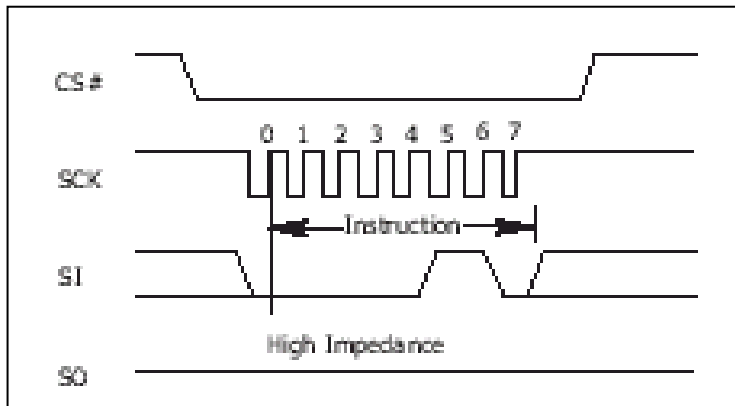


Figure 4 Write Enable (WREN) Instruction Sequence

Write Disable (WRDI)

The Write Disable (WRDI) instruction ([Figure 5](#)) resets the Write Enable Latch (WEL) bit. The Write Disable (WRDI) instruction is entered by driving Chip Enable (CE_L) Low, sending the instruction code, and then driving Chip Enable (CE_L) High.

The Write Enable Latch (WEL) bit is reset under the following conditions:

- Power-up
- Write Disable (WRDI) instruction completion
- Write Status Register (WRSR) instruction completion
- Page Program (PP) instruction completion
- Sector Erase (SE) instruction completion
- Bulk Erase (BE) instruction completion

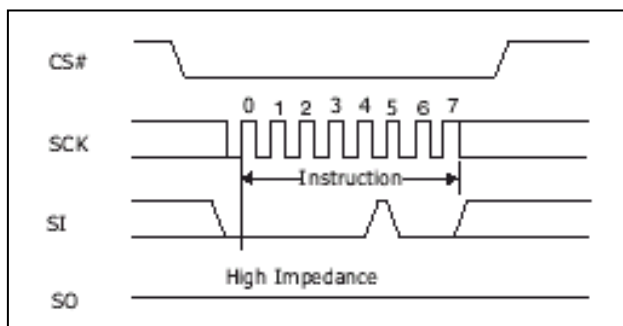


Figure 5 Write Disable (WRDI) Instruction Sequence

Read Status Register (RDSR)

The Read Status Register (RDSR) instruction allows the Status Register to be read. The Status Register may be read at any time, even while a Program, Erase, or Write Status Register cycle is in progress. When one of these cycles is in progress, it is recommended to check the Write In Progress (WIP) bit before sending a new instruction to the device. It is also possible to read the Status Register continuously, as shown in [Figure 6](#).

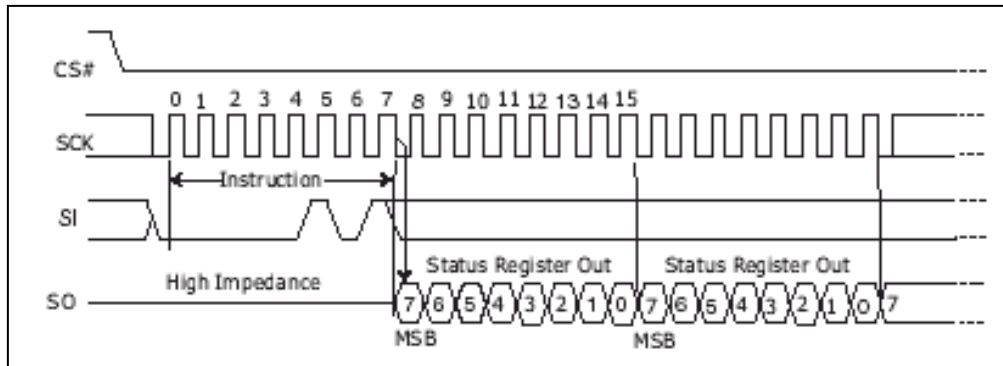


Figure 6 Read Status Register (RDSR) Instruction Sequence

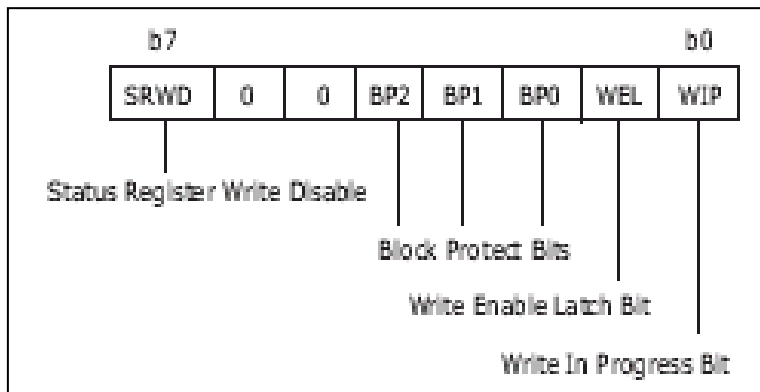


Figure 7 Status Register Format

The status and control bits of the Status Register are as follows:

SRWD bit: The Status Register Write Disable (SRWD) bit is operated in conjunction with the Write Protect (W#) signal. The Status Register Write Disable (SRWD) bit and Write Protect (W#) signal allow the device to be put in the Hardware Protected mode (when the Status Register Write Disable (SRWD) bit is set to 1, and Write Protect (W#) is driven Low). In this mode, the non-volatile bits of the Status Register (SRWD, BP2, BP1, BP0) become read-only bits and the Write Status Register (WRSR) instruction is no longer accepted for execution.

BP2, BP1, BP0 bits: The Block Protect (BP2, BP1, BP0) bits are non-volatile. They define the size of the area to be software protected against Program and Erase instructions. These bits are written with the Write Status Register (WRSR) instruction. When one or both of the Block Protect (BP2, BP1, BP0) bits is set to 1, the relevant memory area ([Table 2](#)) becomes protected against Page Program (PP), and Sector Erase (SE) instructions. The Block Protect (BP2, BP1, BP0) bits can be written provided that the Hardware Protected mode has not been set. The Bulk Erase (BE) instruction is executed if, and only if, all Block Protect (BP2, BP1, BP0) bits are 0.

WEL bit: The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch. When set to 1, the internal Write Enable Latch is set; when set to 0, the internal Write Enable Latch is reset and no Write Status Register, Program or Erase instruction is accepted.

WIP bit: The Write In Progress (WIP) bit indicates whether the memory is busy with a Write Status Register, Program or Erase cycle. This bit is a read only bit and is read by executing a RDSR instruction. If this bit is 1, such a cycle is in progress, if it is 0, no such cycle is in progress.

Write Status Register (WRSR)

The Write Status Register (WRSR) instruction allows new values to be written to the Status Register. Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded and executed, the device sets the Write Enable Latch (WEL). The Write Status Register (WRSR) instruction is entered by driving Chip Enable (CE_L) Low, followed by the instruction code ([Figure 8](#)) and the data byte on Serial Data Input (SI).

The Write Status Register (WRSR) instruction has no effect on bits b6, b5, b1 and b0 of the Status Register. Bits b6 and b5 are always read as 0.

Chip Enable (CE_L) must be driven High after the eighth bit of the data byte has been latched in. If not, the Write Status Register (WRSR) instruction is not executed. As soon as Chip Enable (CE_L) is driven High, the self-timed Write Status Register cycle (whose duration is t_W) is initiated. While the Write Status Register cycle is in progress, the Status Register may still be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Write Status Register cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) is reset.

The WRSR instruction enables the user to select one of seven levels of protection. Each FLASH in the 32MB08SF is divided into eight array segments. The top thirty-second, sixteenth, eighth, quarter, half or all of the memory segments can be protected (as defined in Table 1). The data within a selected segment is therefore read-only. The Write Status Register (WRSR) instruction also allows the user to set or reset the Status Register Write Disable (SRWD) bit in accordance with the Write Protect (W#) signal. The Status Register Write Disable (SRWD) bit and Write Protect (W#) signal allow the device to be put in the Hardware Protected Mode (HPM). The Write Status Register (WRSR) instruction cannot be executed once the Hardware Protected Mode (HPM) is entered.

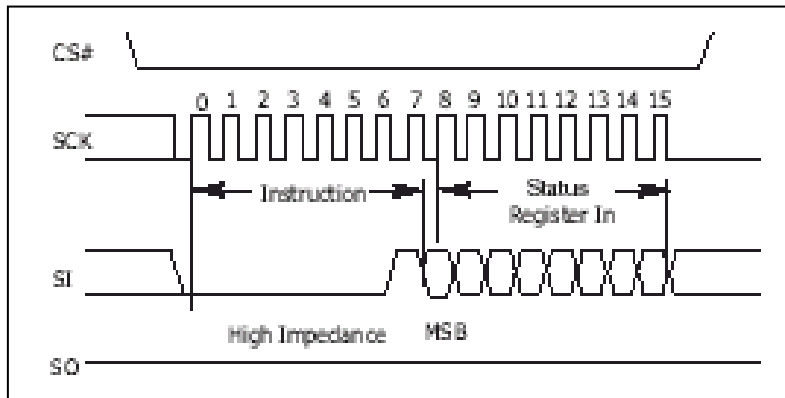


Figure 8 Write Status Register (WRSR) Instruction Sequence

Table 6 Protection Modes

W# Signal	SRWD Bit	Mode	Write Protection of the Status Register	Protected Area (See Note)	Unprotected Area (See Note)
1	1	Software Protected (spm)	Status Register is Writable (if the WREN instruction has set the WEL bit)	Protected against Page Program and Erase (SE, BE)	Ready to accept Page Program and Sector Erase Instructions
1	0		The values in the SRWD, BP2, BP1 BPO bits can be changed		
0	0				
0	1	Hardware Protected (HPM)	Status Register is Hardware write protected The values in the SRWD, BP2, BP1 BPO bits cannot be changed	Protected against P Page Program and Erase (SE, BE)	Ready to accept Page Program and Sector Erase Instructions

Note: As defined by the values in the Block Protect (BP2, BP1, BP0) bits of the Status Register as shown in Table 2.

The protection features of the device are summarized in [Table 6](#). When the Status Register Write Disable (SRWD) bit of the Status Register is 0 (its initial delivery state), it is possible to write to the Status Register provided that the Write Enable Latch (WEL) bit has previously been set by a Write Enable (WREN) instruction, regardless of the whether Write Protect (W#) is driven High or Low.

When the Status Register Write Disable (SRWD) bit of the Status Register is set to 1, two cases need to be considered, depending on the state of Write Protect (W#):

- If Write Protect (W#) is driven High, it is possible to write to the Status Register provided that the Write Enable Latch (WEL) bit has previously been set by a Write Enable (WREN) instruction.
- If Write Protect (W#) is driven Low, it is not possible to write to the Status Register even if the Write Enable Latch (WEL) bit has previously been set by a Write Enable (WREN) instruction. (Attempts to write to the Status Register are rejected, and are not accepted for execution). As a consequence, all the data bytes in the memory area that are software protected (SPM) by the Block Protect (BP1, BP0) bits of the Status Register, are also hardware protected against data modification.

Regardless of the order of the two events, the Hardware Protected Mode (HPM) can be entered:

- by setting the Status Register Write Disable (SRWD) bit after driving Write Protect (W#) Low
- or by driving Write Protect (W#) Low after setting the Status Register Write Disable (SRWD) bit.

The only way to exit the Hardware Protected Mode (HPM) once entered is to pull Write Protect (W#) High.

If Write Protect (W#) is permanently tied High, the Hardware Protected Mode (HPM) can never be activated, and only the Software Protected Mode (SPM), using the Block Protect (BP2, BP1, BP0) bits of the Status Register, can be used.

Read Data Bytes (READ)

The READ instruction reads the memory at the specified SCK frequency (fSCK) with a maximum speed of 33 MHz.

The device is first selected by driving Chip Enable (CE_L) Low. The instruction code for the Read Data Bytes (READ) instruction is followed by a 3-byte address (A23- A0), each bit being latched-in during the rising edge of Serial Clock (SCK). Then the memory contents, at that address, are shifted out on Serial Data Output (SO), each bit being shifted out, at a frequency fSCK, during the falling edge of Serial Clock (SCK).

The instruction sequence is shown in Figure 9. The first byte addressed can be at any location. The address automatically increments to the next higher address after each byte of data are shifted out. The whole memory can, therefore, be read with a single Read Data Bytes (READ) instruction. When the highest address is reached, the address counter rolls over to 00000h which allows the read sequence to be continued indefinitely.

The Read Data Bytes (READ) instruction is terminated by driving Chip Enable (CE_L) High. Chip Enable (CE_L) can be driven High at any time during data output. Any Read Data Bytes (READ) instruction, while a Program, Erase, or Write cycle is in progress, is rejected without having any effect on the cycle that is in progress.

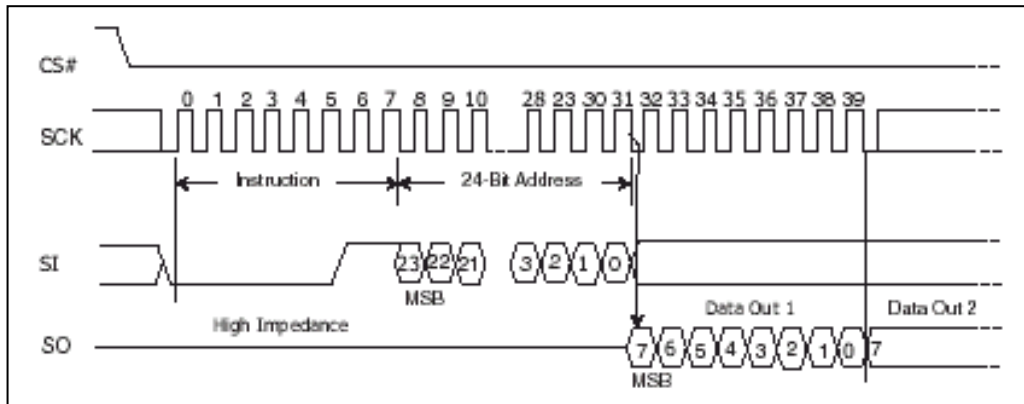


Figure 9. Read Data Bytes (READ) Instruction Sequence

Read Data Bytes at Higher Speed (FAST_READ)

The FAST_READ instruction reads the memory at the specified SCK frequency (fSCK) with a maximum speed of 50 MHz. The device is first selected by driving Chip Enable (CE_L) Low. The instruction code for (FAST_READ) instruction is followed by a 3-byte address (A23-A0) and a dummy byte, each bit being latched in during the rising edge of Serial Clock (SCK). Then the memory contents, at that address, are shifted out on Serial Data Output (SO), each bit being shifted out, at a maximum frequency fSCK, during the falling edge of Serial Clock (SCK).

The instruction sequence is shown in Figure 10. The first byte addressed can be at any location. The address automatically increments to the next higher address after each byte of data are

shifted out. The whole memory can, therefore, be read with a single (FAST_READ) instruction. When the highest address is reached, the address counter rolls over to 00000h, allowing the read sequence to be continued indefinitely.

The (FAST_READ) instruction is terminated by driving Chip Enable (CE_L) High. Chip Enable (CE_L) can be driven High at any time during data output. Any (FAST_READ) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

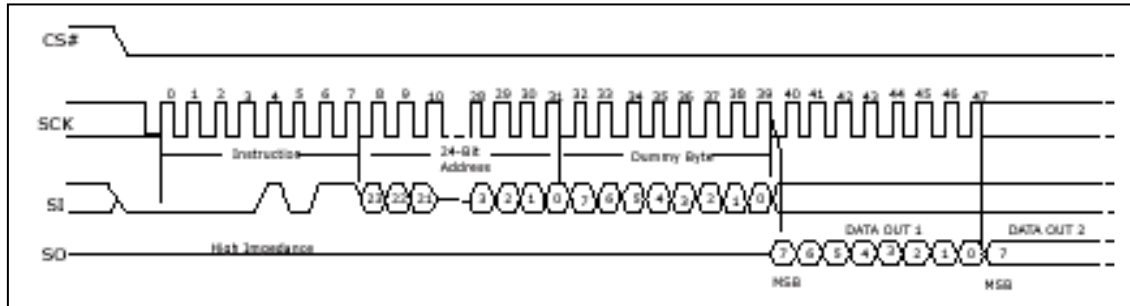


Figure 10. Read Data Bytes at Higher Speed (FAST_READ) Instruction Sequence

Page Program (PP)

The Page Program (PP) instruction allows bytes to be programmed in the memory (changing bits from 1 to 0). Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL).

The Page Program (PP) instruction is entered by driving Chip Enable (CE_L) Low, followed by the instruction code, three address bytes and at least one data byte on Serial Data Input (SI). Chip Enable (CE_L) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in [Figure 11](#).

If more than 256 bytes are sent to the device, the addressing will wrap to the beginning of the same page, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If fewer than 256 Data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page.

Chip Enable (CE_L) must be driven High after the eighth bit of the last data byte has been latched in, otherwise the Page Program (PP) instruction is not executed. As soon as Chip Enable (CE_L) is driven High, the self-timed Page Program cycle (whose duration is t_{PP}) is initiated. While the Page Program cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Page Program (PP) instruction applied to a page that is protected by the Block Protect (BP2, BP1, and BP0) bits (Table 2,) is not executed.

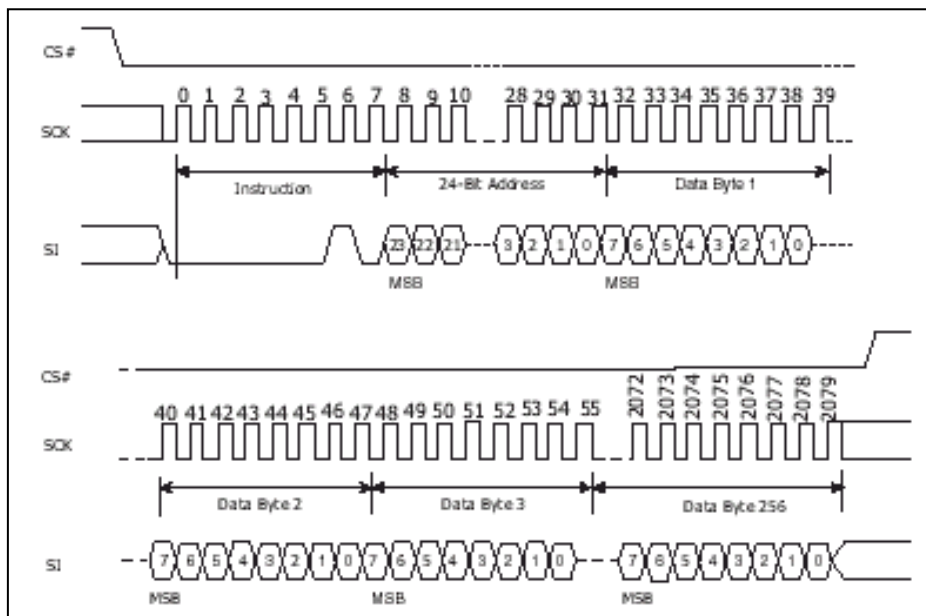


Figure 11. Page Program (PP) Instruction Sequence

Sector Erase (SE)

The Sector Erase (SE) instruction sets to 1 (FFh) all bits inside the chosen sector. Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL).

The Sector Erase (SE) instruction is entered by driving Chip Enable (CE_L) Low, followed by the instruction code, and three address bytes on Serial Data Input (SI). Any address inside the Sector ([Table 2](#),) is a valid address for the Sector Erase (SE) instruction. Chip Enable (CE_L) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in [Figure 12](#).

Chip Enable (CE_L) must be driven High after the eighth bit of the last address byte has been latched in, otherwise the Sector Erase (SE) instruction is not executed. As soon as Chip Enable (CE_L) is driven High, the self-timed Sector Erase cycle (whose duration is tSE) is initiated. While the Sector Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Sector Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Sector Erase (SE) instruction applied to any memory area that is protected by the Block Protect (BP2, BP1, BP0) bits ([Table 2](#)) is not executed.

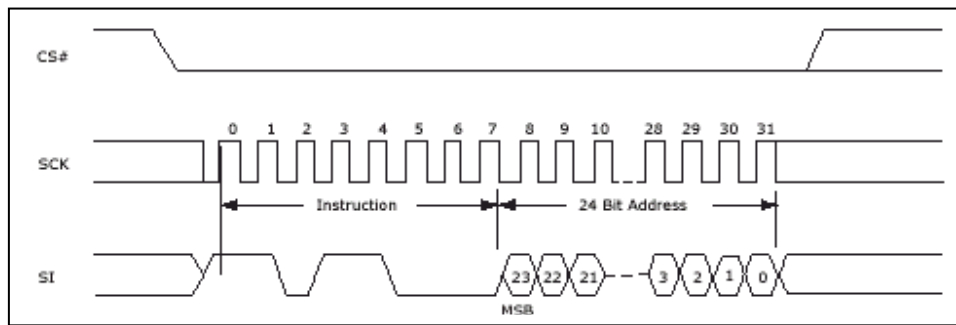


Figure 12. Sector Erase (SE) Instruction Sequence

Bulk Erase (BE)

The Bulk Erase (BE) instruction sets to 1 (FFh) all bits inside the entire memory. Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL).

The Bulk Erase (BE) instruction is entered by driving Chip Enable (CE_L) Low, followed by the instruction code, on Serial Data Input (SI). No address is required for the Bulk Erase (BE) instruction. Chip Enable (CE_L) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in [Figure 13](#).

Chip Enable (CE_L) must be driven High after the eighth bit of the last address byte has been latched in, otherwise the Bulk Erase (BE) instruction is not executed.

As soon as Chip Enable (CE_L) is driven High, the self-timed Bulk Erase cycle (whose duration is tBE) is initiated. While the Bulk Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Bulk Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Bulk Erase (BE) instruction is executed only if all the Block Protect (BP2, BP1, BP0) bits (see [Table 2](#)) are set to 0. The Bulk Erase (BE) instruction is ignored if one or more sectors are protected.

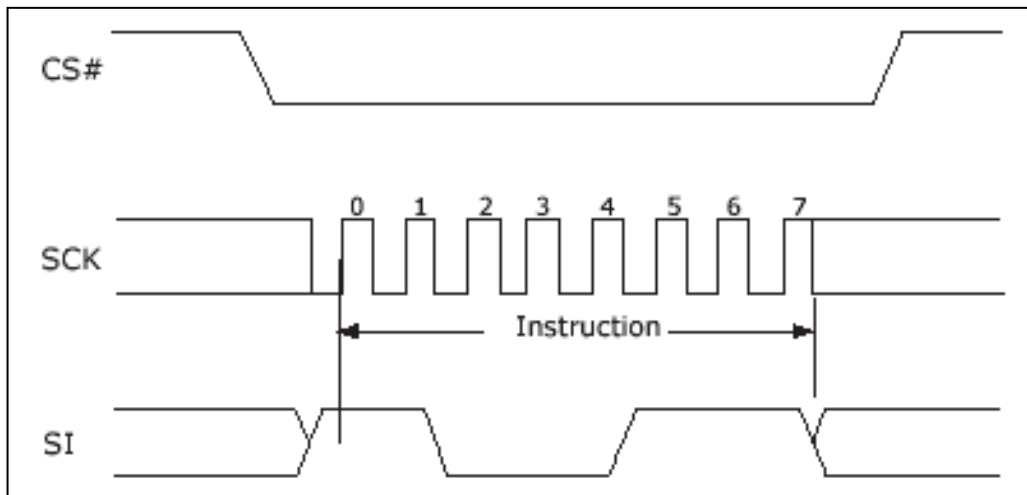


Figure 13. Bulk Erase (BE) Instruction Sequence

Deep Power Down (DP)

The Deep Power Down (DP) instruction puts the device in the lowest current mode of 1 μ A typical.

It is recommended that the standard Standby mode be used for the lowest power current draw, as well as the Deep Power Down (DP) as an extra software protection mechanism when this device is not in active use. In this mode, the device ignores all Write, Program and Erase instructions. Chip Enable (CE_L) must be driven Low for the entire duration of the sequence.

The Deep Power Down (DP) instruction is entered by driving Chip Enable (CE_L) Low, followed by the instruction code on Serial Data Input (SI). Chip Enable (CE_L) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in [Figure 14](#).

Driving Chip Enable (CE_L) High after the eighth bit of the instruction code has been latched puts the device in Deep Power Down mode. The Deep Power Down mode can only be entered by executing the Deep Power Down (DP) instruction to reduce the standby current (from ISB to IDP as specified in [Table 8](#)). As soon as Chip Enable (CE_L) is driven high, it requires a delay of tDP currently in progress before Deep Power Down mode is entered.

Once the device has entered the Deep Power Down mode, all instructions are ignored except the Release from Deep Power Down (RES) and Read Electronic Signature. This releases the device from the Deep Power Down mode. The Release from Deep Power Down and Read Electronic Signature (RES) instruction also allows the Electronic Signature of the device to be output on Serial Data Output (SO).

The Deep Power Down mode automatically stops at Power-down, and the device always powers up in the Standby mode. Any Deep Power Down (DP) instruction, while an Erase, Program or WRSR cycle is in progress, is rejected without having any effect on the cycle in progress.

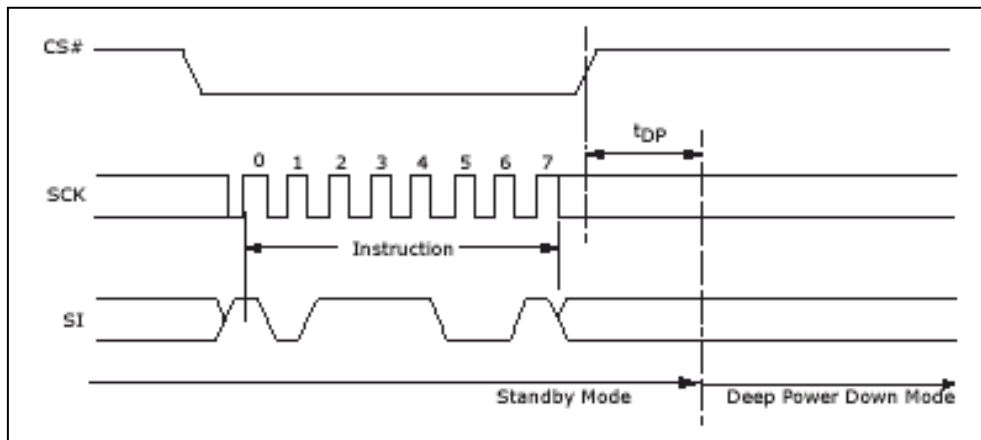


Figure 14. Deep Power Down (DP) Instruction Sequence

Release from Deep Power Down (RES)

The Release from Deep Power Down (RES) instruction provides the only way to exit the Deep Power Down mode. Once the device has entered the Deep Power Down mode, all instructions are ignored except the Release from Deep Power Down (RES) instruction. Executing this instruction takes the device out of Deep Power Down mode.

The Release from Deep Power Down (RES) instruction is entered by driving Chip Enable (CE_L) Low, followed by the instruction code on Serial Data Input (SI). Chip Enable (CE_L) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in [Figure 15](#).

Driving Chip Enable (CE_L) High after the 8-bit instruction byte has been received by the device, but before the whole of the 8-bit Electronic Signature has been transmitted for the first time, still insures that the device is put into Standby mode. If the device was previously in the Deep Power Down mode, though, the transition to the Stand-by Power mode is delayed by t_{RES} , and Chip Enable (CE_L) must remain High for at least $t_{RES(max)}$, as specified in [Table 10](#). Once in the Stand-by Power mode, the device waits to be selected, so that it can receive, decode and execute instructions.

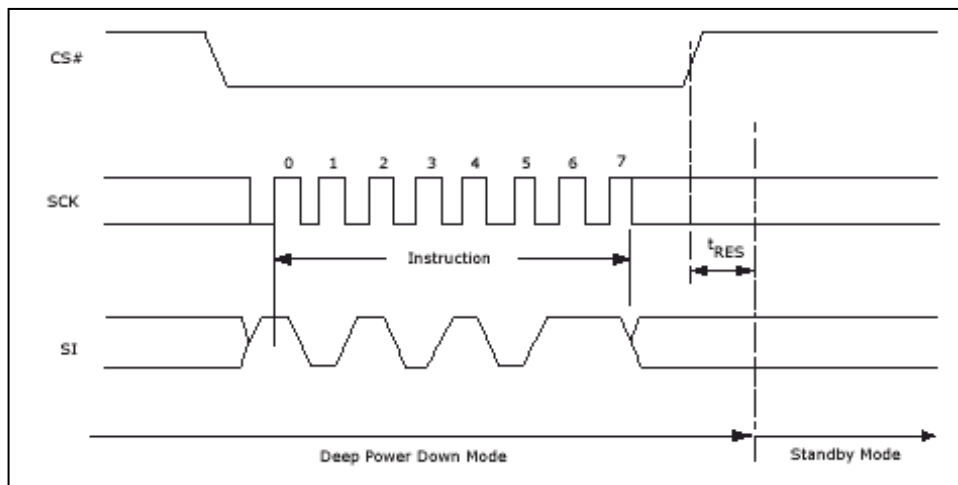


Figure 15. Release from Deep Power Down Instruction Sequence

Release from Deep Power Down and Read Electronic Signature (RES)

Once the device has entered Deep Power Down mode, all instructions are ignored except the RES instruction. The RES instruction can also be used to read the oldstyle 8-bit Electronic Signature of the device on the SO pin. The RES instruction always provides access to the Electronic Signature of the device (except while an Erase, Program or WRSR cycle is in progress), and can be applied even if DP mode has not been entered. Any RES instruction executed while an Erase, Program or WRSR cycle is in progress is not decoded, and has no effect on the cycle in progress. The device features an 8-bit Electronic Signature, whose value for the 32MB08SF is 14h. This can be read using RES instruction.

The device is first selected by driving Chip Enable (CE_L) Low. The instruction code is followed by three dummy bytes, each bit being latched-in on Serial Data Input (SI) during the rising edge of Serial Clock (SCK). Then, the 8-bit Electronic Signature, stored in the memory, is shifted out on Serial Data Output (SO), each bit being shifted out during the falling edge of Serial Clock (SCK). The instruction sequence is shown in Figure 16.

The Release from Deep Power Down and Read Electronic Signature (RES) is terminated by driving Chip Enable (CE_L) High after the Electronic Signature has been read at least once. Sending additional clock cycles on Serial Clock (SCK), while Chip Enable (CE_L) is driven Low, causes the Electronic Signature to be output repeatedly.

When Chip Enable (CE_L) is driven High, the device is put in the Stand-by Power mode. If the device was not previously in the Deep Power Down mode, the transition to the Stand-by Power mode is immediate. If the device was previously in the Deep Power Down mode, though, the transition to the Standby mode is delayed by tRES, and Chip Enable (CE_L) must remain High for at least tRES(max), as specified in Table 10. Once in the Stand-by Power mode, the device waits to be selected, so that it can receive, decode and execute instructions.

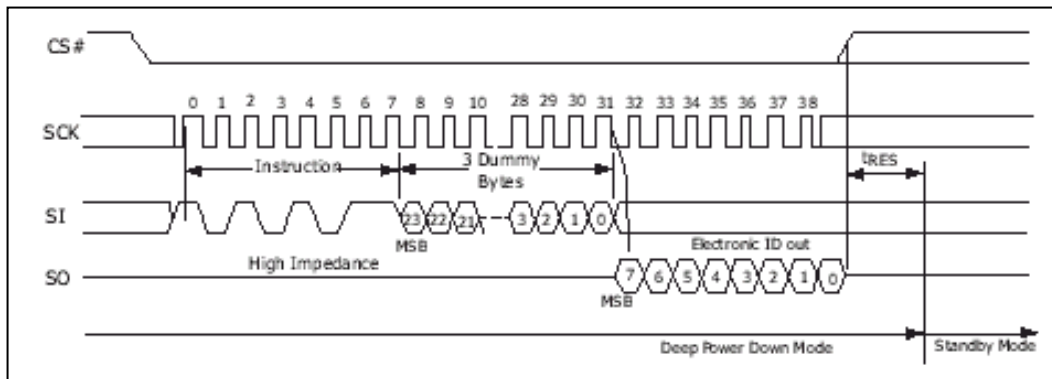


Figure 16. Release from Deep Power Down and Read Electronic Signature (RES) Instruction Sequence

Power-up and Power-down

The device must not be selected at power-up or power-down (that is, CE_L must follow the voltage applied on VCC) until VCC reaches the correct value as follows:

- VCC (min) at power-up, and then for a further delay of tPU (Table 7)
- VSS at power-down

A simple pull-up resistor on Chip Enable (CE_L) can usually be used to insure safe and proper power-up and power-down.

The device ignores all instructions until a time delay of tPU (Table 7) has elapsed after the moment that VCC rises above the minimum VCC threshold. However, correct operation of the device is not guaranteed if by this time VCC is still below VCC (min). No Write Status Register, Program or Erase instructions should be sent until tPU after VCC reaches the minimum VCC threshold.

At power-up, the device is in Standby mode (not Deep Power Down mode) and the WEL bit is reset.

Normal precautions must be taken for supply rail decoupling to stabilize the VCC feed. Each device in a system should have the VCC rail decoupled by a suitable capacitor close to the package pins (this capacitor is generally of the order of 0.1 μ F).

At power-down, when VCC drops from the operating voltage to below the minimum VCC threshold, all operations are disabled and the device does not respond to any instructions. (The designer needs to be aware that if a power-down occurs while a Write, Program or Erase cycle is in progress, data corruption can result.)

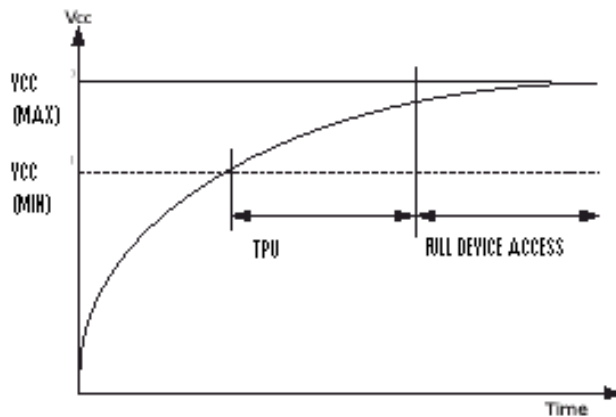


Figure 17 Power-Up Timing

Table 7. Power-Up Timing

Symbol	Parameter	Min.	Max.	Unit
Vcc (min)	Vcc (minimum)	2.07		V
	Vcc (min) to device operation	10		mSec

Initial Delivery State

The device is delivered with all bits set to 1 (each byte contains FFh). The Status Register contains 00h (all Status Register bits are 0).

Maximum Rating

Stressing the device above the rating listed in the **Absolute Maximum Ratings** section below may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Absolute Maximum Ratings

Voltage with Respect to Ground:

All Inputs and I/Os. -0.3 V to 4.5 V

Operating Ranges

Positive Power Supply

Voltage Range 2.7 V to 3.6 V

Temperature. 175 degrees Celsius

Note: Operating ranges define those limits between which functionality of the device is guaranteed.

DC Characteristics

This section summarizes the DC and AC Characteristics of the individual memory devices in the 32MB08SF. There are 32 individual memory devices in the 32MB08SF. Designers should check that the operating conditions in their circuit match the measurement conditions specified in the Test Specifications in [Table 9](#), when relying on quoted parameters. The characteristics

CMOS Compatible

Table 8

Parameter	Description	Test Conditions (See Note)		Min.	Typ.	Max	Unit
Vcc	Supply Voltage			2.7	3	3.6	V
Icc1	Active Read Current	SCK=0.1V _c c/0.9V _{cc}	33MHz		9	12	mA
		SCK=0.1 V _{cc} /0.9V _{cc}	V _{cc} =3.0 50 MHz		14	19	mA
Icc2	Active Page Program Current	CE_L=Vcc			19	24	mA
Icc3	Active WRSR Current	CE_L=Vcc				24	mA
Icc4	Active Sector Erase Current	CE_L=Vcc				24	mA
Icc5	Active Bulk Erase Current	CE_L=Vcc				24	mA
Isb	Standby Current	V _{cc} =3.0V CE_L=Vcc			21	50	uA
Idp	Deep Power Down Current	V _{cc} =3.0V CE_L=Vcc			1.3	5	uA
Ili	Input Leakage Current	VIN=GND to Vcc				1	uA
Ilo	Output Leakage Current	VIN=GND to Vcc				1	uA
Vil	Input Low Voltage			-0.3		0.3V _{cc}	V
Vih	Input High Voltage			0.7V _{cc}		V _{cc} +0.5	V
Vol	Output Low Voltage	IOL=1.6 mA, V _{cc} +V _{cc} min				0.4	V
VoH	Output High Voltage	IOH=-0.1 mA		V _{cc} -0.2			V

Test Conditions

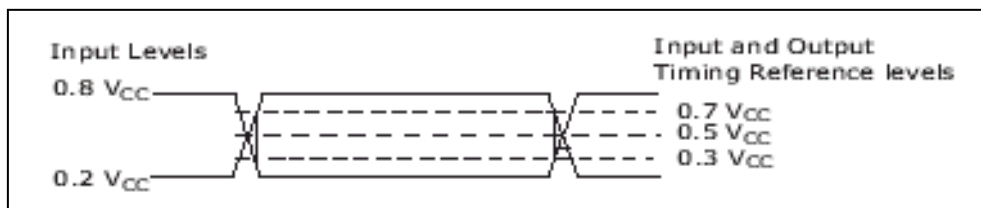


Figure 18 AC Measurements I/O Waveform

Table 9 Test Specifications

Symbol	Parameter	Min	Max	Unit
C1	Load Capacitance		30	pF
	Input Rise and Fall Times		5	ns
	Input Pulse Voltage	0.2 Vcc to 0.8 Vcc		V
	Input Timing Reference Voltage	0.3 Vcc to 0.7 Vcc		V
	Output Timing reference Voltage	0.5 Vcc		V

AC Characteristics

Table 10. AC Characteristics

Symbol (Notes)	Parameter	Min	Typ (Notes)	Max (Notes)	Unit
FCK	SCK Clock Frequency READ instruction	D.C.		33	MHz
FCK	SCK Clock Frequency for: Fast_READ, PP, SE, BE, DP, RES, WREN, WRDI, RDSR, WRSR	D.C.		50	MHz
TCRT	Clock Rise Time (Slew Rate)	0.1			V/ns
TCFT	Clock Fall Time (Slew Rate)	0.1			V/ns
TWH	SCK High Time	9			ns
TWL	SCK Low Time	9			ns
TCS	CE_L High Time	100			ns
TCSS(3)	CE_L Setup time	5			ns
TCSH(3)	CE_L Hold Time	5			ns
THD(3)	Hold# Setup Time (relative to SCK)	5			ns
TCD(3)	Hold# Hold Time (relative to SCK)	5			ns
THC	Hold# Setup Time (relative to SCK)	5			ns
TCH	Hold# Setup Time (relative to SCK)	5			ns
TV	Output Valid			10	ns
THO	Output Hold Time	0			ns
THD:DAT	Data in Hold Time	5			ns
TSU:DAT	Data in Setup Time	5			ns
TR	Input Rise Time			5	ns
TF	Input Fall Time			5	ns
TLZ	Hold# to Output Low Z			10	ns
THZ	Hold# to output High Z			10	ns
TDIS	Output Disable Time			10	ns
TWPS	Write Protect Setup Time	15			ns
TWPH	Write Protect Hold Time	15			ns
TW	Write Status Register Time			65	ms
TDP	CE_L High to Deep Power Down Mode			3	us
TRES	Release DP Mode			30	us
TPP	Page Programming Time		1.4(1)	3(2)	ms
TSE	Sector Erase Time		0.5(1)	3(2)	sec
TBE	Bulk Erase Time		1.4(1)	96(2)	sec

Notes:

1. Typical program and erase times assume the following conditions: 25°C, VCC = 3.0V; 10,000 cycles; checkerboard data pattern
2. Under worst-case conditions of 90°C; VCC = 2.7V; 100,000 cycles
3. Not 100% tested

AC Characteristics

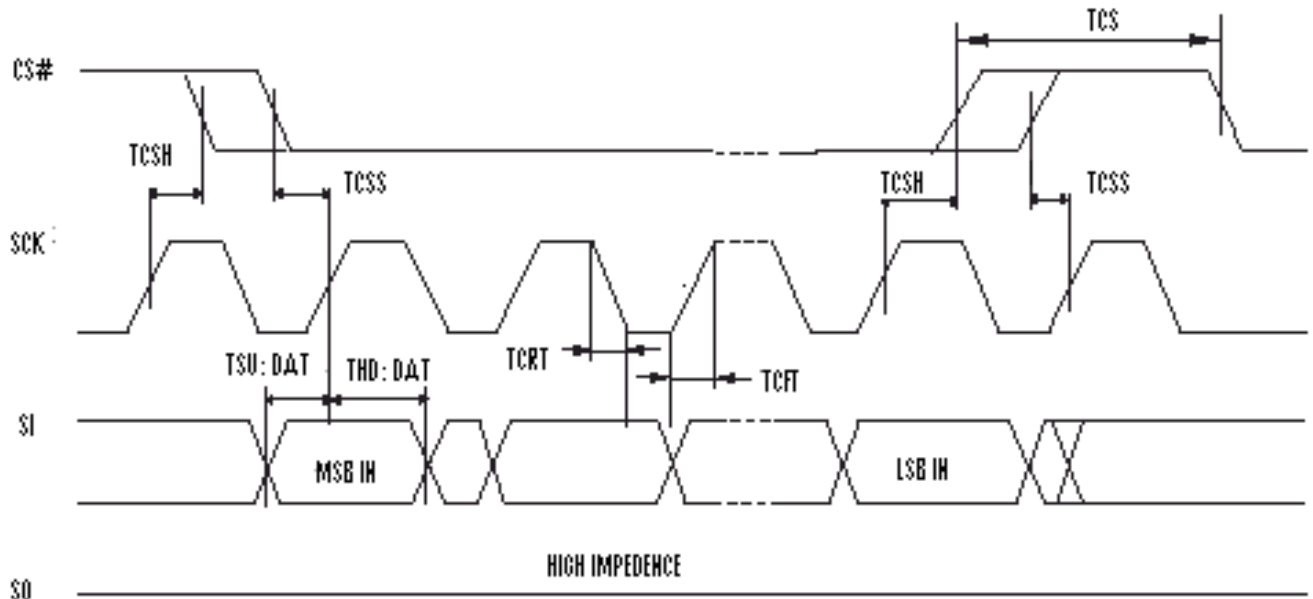


Figure 19 SPI Mode 0 (0,0) Input Timing

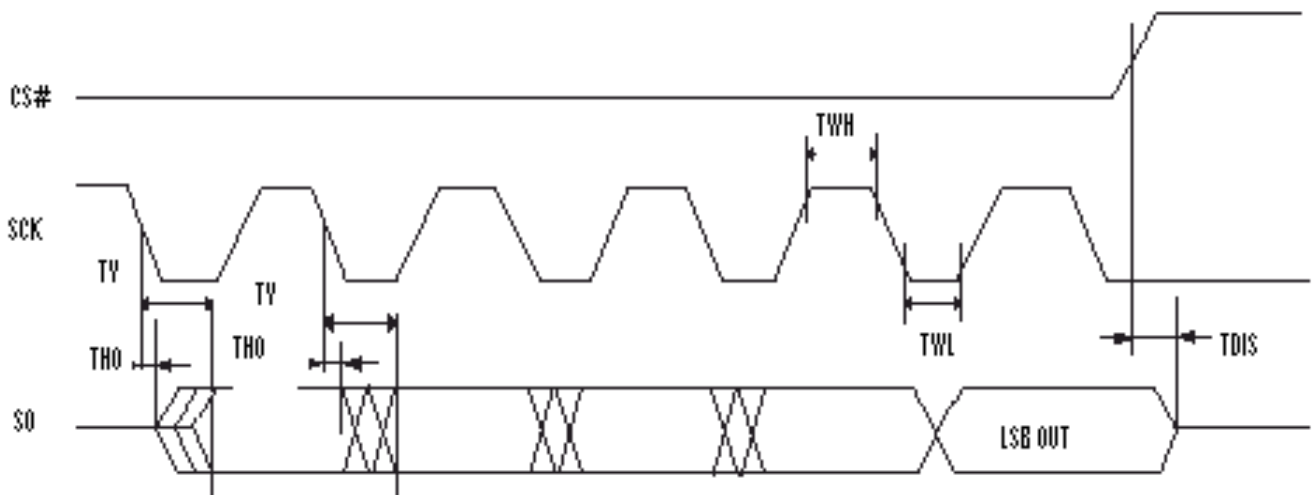


Figure 20 SPI Mode 0 (0,0) Output Timing

AC Characteristics

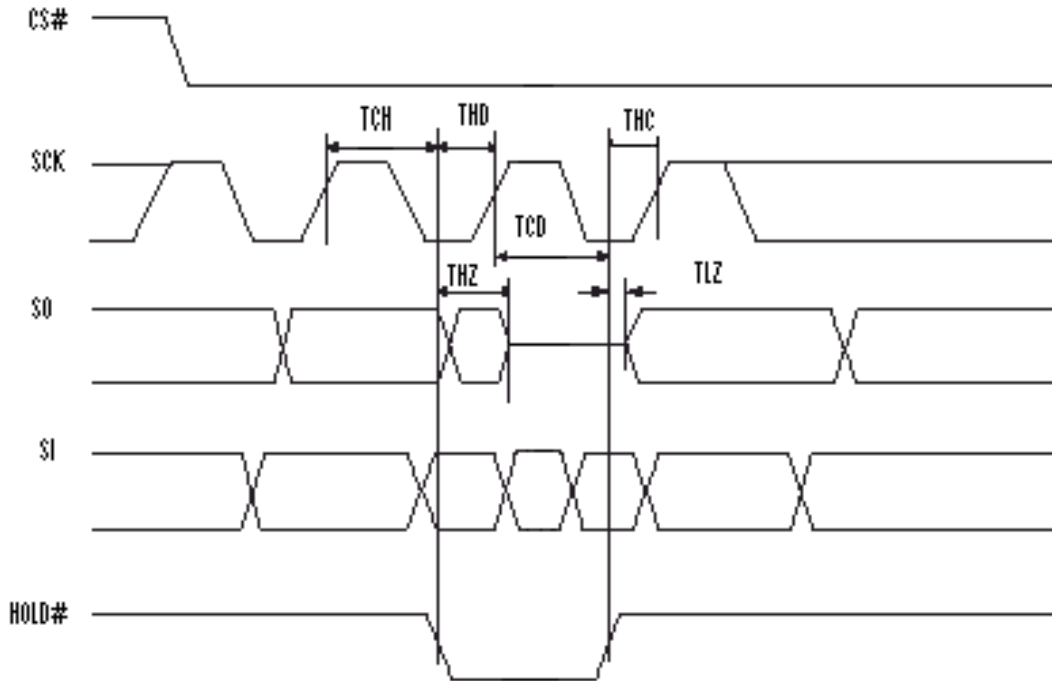


Figure 21 HOLD# Timing

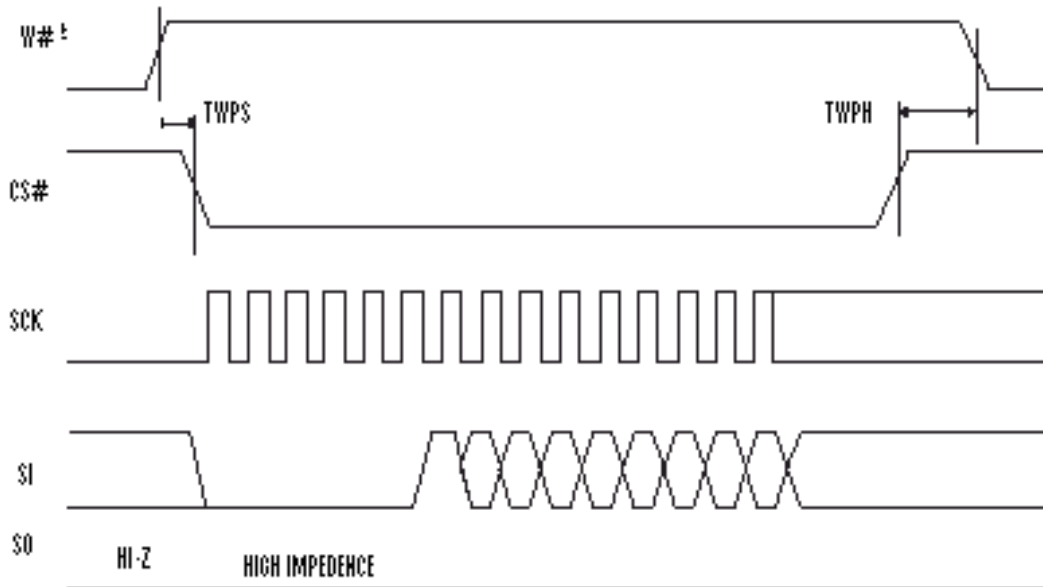


Figure 22 Write Protect Setup and Hold Timing during WRSR when SRWD=1

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Document

Revision History

Revision No.	Description	Date
1.0	Initial Release – Advance Information	16 September 2006
2.0	Mechanical drawing added	9 January 2009
2.1	Advance information comments removed	27 October 2009
2.2	Corrected some legibility problems	27 April 2010