

230 S. Siesta Lane

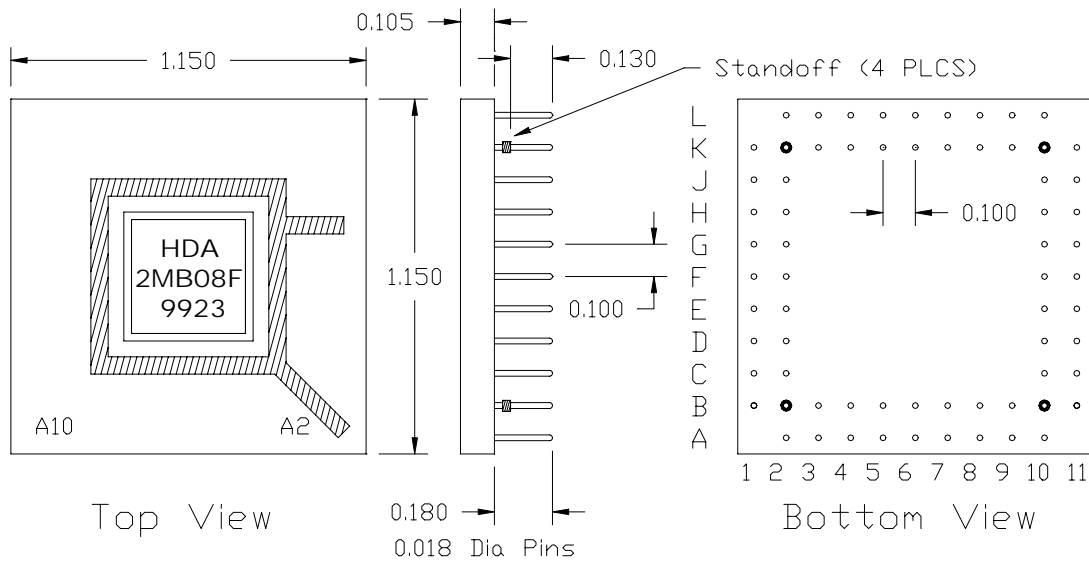
Tempe, AZ 85281

Fax: 480-894-2578

High Temperature 2MB Flash Memory Module

Part Number 2MB08F-01

CMOS 5.0 Volt-only 8-bit



CHARACTERISTICS

- 5.0 VOLT +/- 10% FOR READ AND WRITE OPERATIONS
- SECTOR ERASE ARCHITECTURE
- SUPPORTS FULL CHIP ERASE
- EMBEDDED ERASE ALGORITHMS
- EMBEDDED PROGRAM ALGORITHMS
- DATA POLLING AND TOGGLE BIT FEATURE FOR DETECTION OF PROGRAM OR ERASE CYCLE COMPLETION
- READY/BUSY OUTPUT (FLASHRDY) HARDWARE DETECTION OF PROGRAM OR ERASE CYCLE COMPLETION
- ERASE SUSPEND/RESUME SUPPORTS READING OR PROGRAMMING DATA TO A SECTOR NOT BEING ERASED
- LOW POWER CONSUMPTION
- HARDWARE RESET PIN TO SET INTERNAL STATE MACHINE TO THE READ MODE
- DESIGNED FOR HIGH TEMPERATURE APPLICATIONS

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Pin	Description	Pin	Description	Pin	Description
A2	A_H5	C11	--	J10	A_H20
A3	A_H6	D1	--	J11	--
A4	A_H8	D2	--	K1	--
A5	A_H10	D10	--	K2	A_H2
A6	RSTFLASH_L	D11	--	K3	A_H0
A7	CE_L	E1	--	K4	D_H1
A8	A_H13	E2	--	K5	D_H3
A9	A_H15	E10	--	K6	VSS - GND
A10	A_H17	E11	--	K7	D_H4
B1	--	F1	--	K8	D_H6
B2	--	F2	VSS - GND	K9	FLASHRDY_H
B3	A_H7	F10	VSS - GND	K10	--
B4	A_H9	F11	--	K11	--
B5	A_H11	G1	--	L2	A_H1
B6	VCC - 5 Volts	G2	--	L3	D_H0
B7	A_H12	G10	--	L4	D_H2
B8	A_H14	G11	--	L5	--
B9	A_H16	H1	--	L6	VCC - 5 Volts
B10	A_H18	H2	--	L7	D_H5
B11	--	H10	--	L8	D_H7
C1	--	H11	--	L9	RE_L
C2	A_H4	J1	--	L10	WE_L
C10	A_H19	J2	A_H3	--	--

Table 1

Signal Description

VCC + 5 Volts	Power Supply
WE_L	Write Enable Asserted Low Input
CE_L	Chip Enable Asserted Low Input
RSTFLASH_L	Reset Flash Asserted Low Input
RE_L	Read/Output Enable Asserted Low Input
FLASHRDY_H	Flash Ready Tristate Output
A_H[20..0]	Address Inputs
D_H[7..0]	Data Input/Outputs
VSS - GND	Ground

Table 2

General Description

The 2MB08F is a 2 megabyte 5.0 Volt-only Flash Memory. The part can be programmed in-system with the standard 5.0 Volt supply. It is not necessary to use a programmer to erase or program the part.

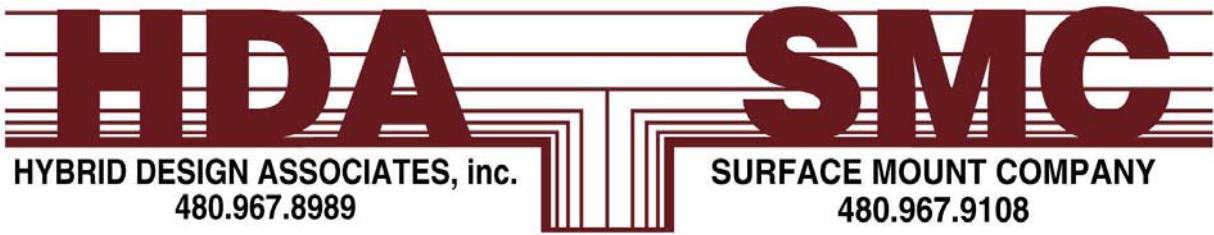
The command set complies with the JEDEC single-power-supply Flash standard. Commands are written to the internal command register using standard microprocessor write timings. The command register is the input to an internal state-machine which controls the erase and programming circuitry. Reading data from the device is similar to reading other flash or EEPROM devices.

An internal programming algorithm automatically programs the device after the programming command sequence is entered. Device erasure occurs by executing the erase command sequence. The internal circuitry automatically times the erase pulse widths and verifies proper cell margin.

The host system detects whether the program or operation is done by monitoring the FLASHRDY pin, or by reading the D_H7 (Polling) and D_H6 Toggle Status bits.

64K byte sectors can be erased and reprogrammed individually without affecting the data contents of other sectors.

The device will not program or erase if the VCC pin is too low. Data from a sector that is

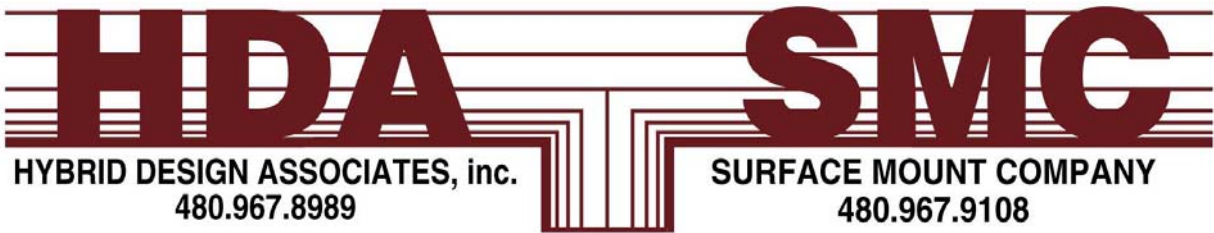


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not participating in a sector erase can be read during the erase process via the Erase Suspend feature.



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The FLASHRST_L pin terminates any operation in progress and resets the internal state machine to reading array data. When the FLASHRST_L pin is held low the device is placed in a low power standby mode to reduce power consumption.

ABSOLUTE MAXIMUM RATINGS

Parameter		Unit
Voltage on Any Pin with Respect to GND (Except VCC)	-2.0 to 7.0	Volts
VCC Supply Voltage with Respect to GND	-2.0 to 7.0	Volts

Table 3

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	VCC	4.7	5.2	Volts
Input High Voltage	Vih	2.0	VCC + 0.5	Volts
Input Low Voltage	Vil	-0.5	0.8	Volts
Operating Temperature	Ta	-55		Degrees C

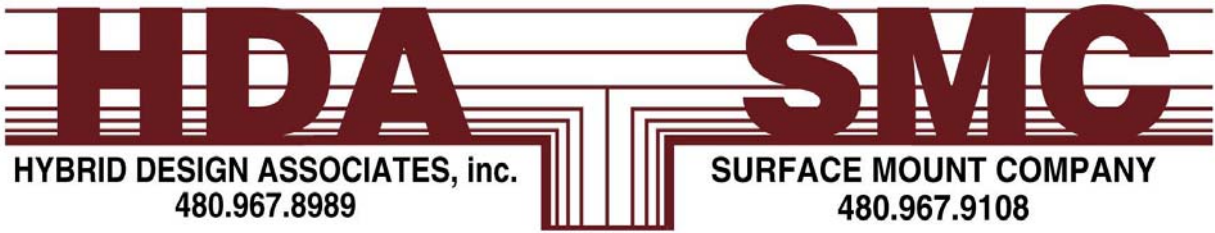
Table 4

CAPACITANCE

(Ta =)

Parameter	Symbol	Conditions	Typ	Unit
RE_L	Cre	Vin=0V, F=1.0 KHz	11	pF
WE_L	Cwe	Vin=0V, F=1.0 KHz	10	pF
CE_L	Cce	Vin=0V, F=1.0 KHz	8	pF
FLASHRDY_H	Cfr	Vin=0V, F=1.0 KHz	10	pF
RSTFLASH_L	Crf	Vin=0V, F=1.0 KHz	9	pF
A_H[20..0]	Cad	Vin=0V, F=1.0 KHz	10	pF
D_H[7..0]	Cio	Vin=0V, F=1.0 KHz	10	pF

Table 5



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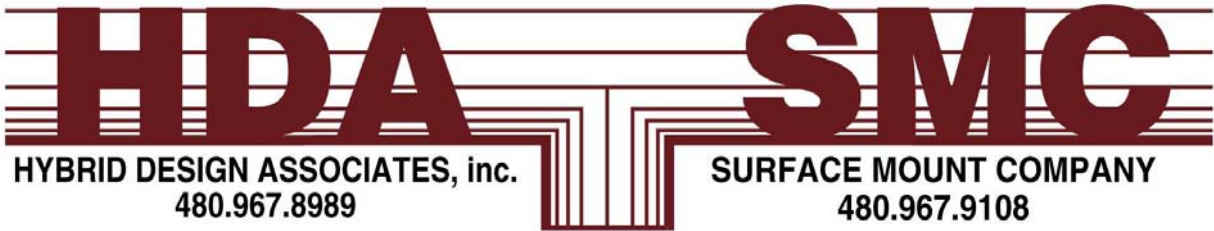
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DC CHARACTERISTICS

Parameter	Symbol	Conditions	Typ	Max	Unit
Input Leakage Current	Ili	VCC=5.5, Vin = VCC to GND		+/- 1.0	uA
Output Leakage Current	Ilo	VCC=5.5, Vout = VCC to GND		+/- 1.0	uA
VCC Standby Current	Iccs	VCC=5.5,RE,WE,CS = GND, RSTFLASH=GND	1	5	uA
VCC Read Current	Iccr	VCC=5.5,CS=GND,RE=GND Iout = 0ma	25	40	mA
VCC Write Current	Iccw	Write in Progress	30	40	mA
VCC Erase Current	Icce	Erase in Progress	30	40	mA
Output Low Voltage	Vol	VCC=4.5, Iol=5.8 mA		0.45	Volts
Output High Voltage	Voh	VCC=4.5,Ioh=-2.5 mA	VCC -0.45		Volts
VCC Erase/Write Lockout Voltage	Vlko		3.2	4.2	Volts

Table 6



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AC CHARACTERISTICS - READ-ONLY OPERATIONS

Parameter	Symbol		Min	Typ	Max	Unit
Read Cycle Time	Tavav	Trc	90	-	-	nS
Address Access Time	Tavqv	Tacc	-	-	90	nS
Chip Select to Output Valid	Telqv	Tce	-	70	90	nS
Output Enable to Output Valid	Tglov	Toe	-	80	95	nS
Chip Select to Output Low Z	Telqz	Tlz	-	13	-	nS
Chip Select High to to Output High Z	Tehqz	Thz	-	5	-	nS
Output Enable to Output Low Z	Tglox	Tqlz	-	25	-	nS
Reset to Output Valid	Tphqv	Tpwh	-	-	50	nS
Output Enable High to Output High Z	Tghqz	Tdf	-	17	20	nS
Output Hold from Address, CS_1 , RE_L Change, or Whichever is First	Toh	Toh	0.0	-	-	nS

Table 7

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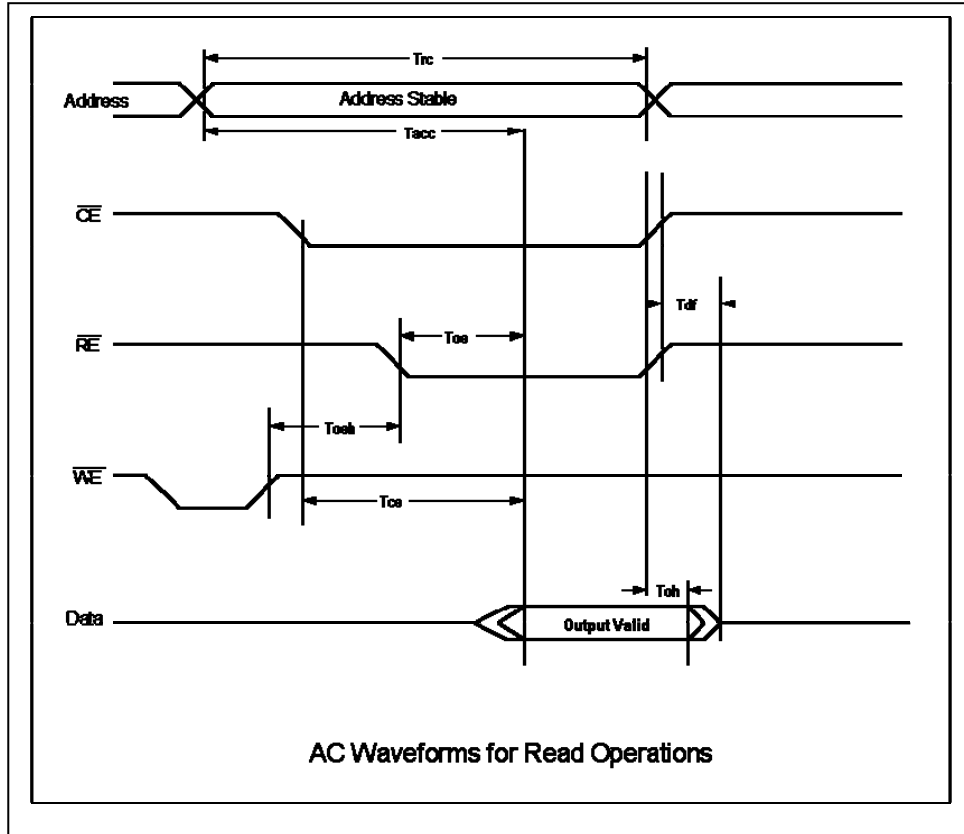
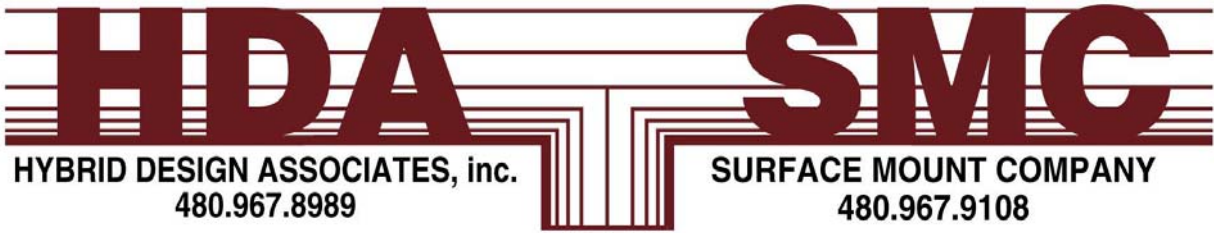


Figure #1



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AC CHARACTERISTICS - WRITE/ERASE/PROGRAM OPERATIONS - WE_L
CONTROLLED

Parameter	Symbol		Min	Typical	Max	Unit
Write Cycle Time	Tavav	Twc	90	-	-	nS
Chip Enable Setup Time	Telwl	Tcs	0	-	-	nS
Write Enable Pulse Width	Twlwh	Twp	45	-	-	nS
Address Setup to WE_L going Low	Tavwh		0	-	-	nS
Data Setup Time	Tdvwh	Tds	45	-	-	nS
Data Hold Time	Twhdx	Tdh	0	-	-	nS
Address Hold Time	Twhax	Tah	45	-	-	nS
Chip Select Hold time	Twheh	Tch	0	-	-	nS
Write Enable Pulse Width High	Twhwl	Twph	20	-	-	nS
Duration of Byte Write Operation	Twhqv1		-	7	-	uS
Duration of Block Erase Operation	Twhqv2		-	1	8	Sec
Duration of Chip Erase Operation	Twhqv3		-	32	256	Sec
Write Recovery Before Read	Twhgl		-	2	-	uS

Table 8

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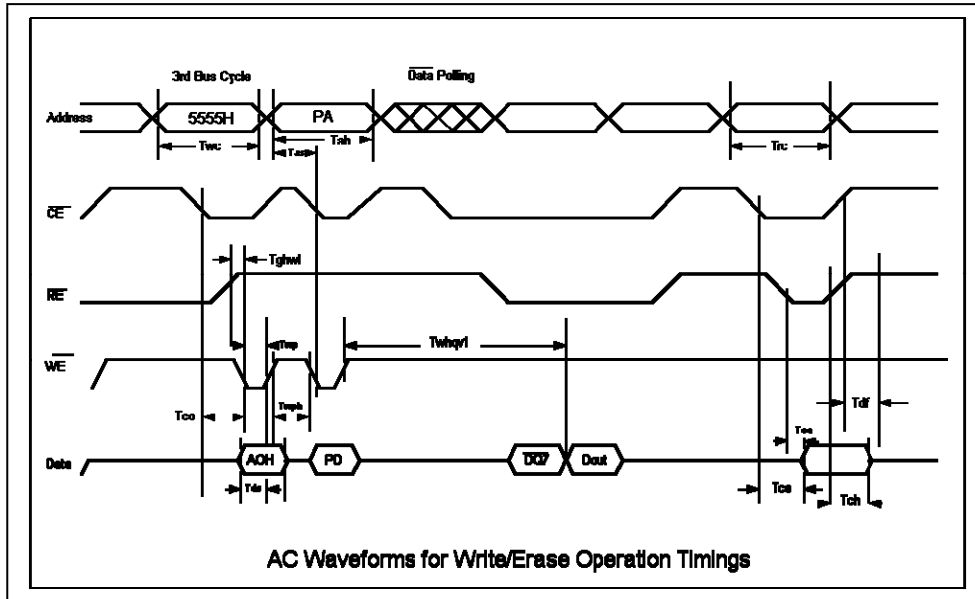
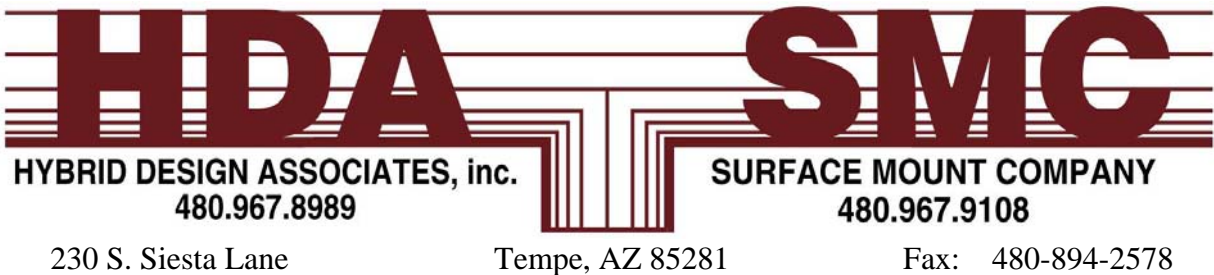


Figure 3

User Bus Operations

Operation	CE_L	RE_L	WE_L	A[20..0]	D[7..0]	Reset
Read	L	L	H	Select	Dout	H
Standby	H	H	X	X	High Z	H
Output Disable	L	H	H	Select	High Z	H
Write	L	H	L	Select	Din	H
Hardware Reset/Standby	H	H	H	X	High Z	L

Table 9



Read Mode

The 2MB08F has two control functions which must be satisfied in order to obtain data at the outputs. The chip select signal `CE_L` must be low, the address lines must be stable and the `RE_L` signal must be low. `RE_L` serves as a tristate enable to enable the data on the lines.

Address access time (T_{acc}) is equal to the delay from stable addresses to valid output data. The chip enable access time (T_{cs}) is the delay from stable addresses and stable `CE_L` to valid data at the output pins. The output enable access time is the delay from the falling edge of `RE_L` to valid data at the output pins assuming the addresses have been stable for at least $T_{acc}-T_{ce}$ time.

Standby Mode

There are two ways to implement a Standby Mode. One is to set `CE_L` to the high state, and the other is to assert the Hardware Reset pin `RSTFLASH_L` to a Low State. When using both signals to implement the Standby mode `CE_L` in the High State, and `RSTFLASH_L` in the low state the current drawn by the device is lowest and is typically 5 or less microAmps. `RE_L` should be in the high state when implementing the Standby Mode.

Output Disable

With the `RE_L` input at a logic high level, output from the device is disabled.

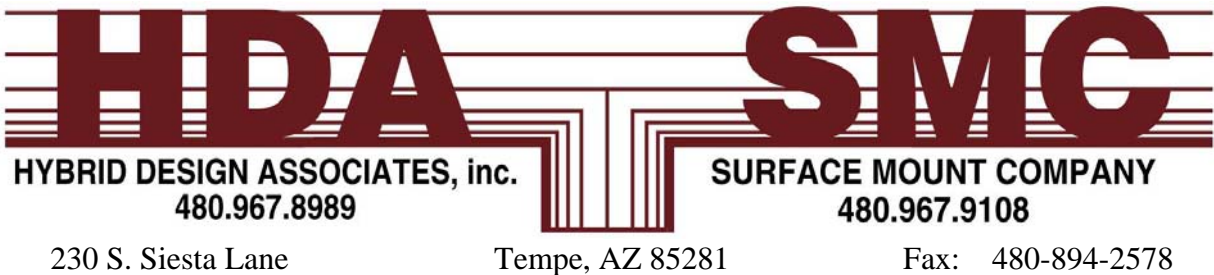
2MB08F Command Definitions

Command Sequence Read/Reset	Bus Write Cycles Required	First Bus Write Cycle		Second Bus Write Cycle		Third Bus Write Cycle		Fourth Bus Read/Write Cycle		Fifth Bus Write Cycle		Sixth Bus Write Cycle	
		ADDR	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Reset/Read	1	xxxxH	F0H										
Reset/Read	3	5555H	AAH	2AAAH	55H	5555H	F0H	RA	RD				
Byte Program	4	5555H	AAH	2AAAH	55H	5555H	A0H	PA	PD				
Chip Erase	6	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	10H
Sector Erase	6	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	SA	30H
Erase Suspend	1	xxxxH	B0H										
Erase Resume	1	xxxxH	30H										

Table 10

Notes:

1. RA = Address of the memory location to be read.
 PA = Address of the memory location to be programmed. Address are latched on the falling edge of the WE_L pulse.
 SA = Address of the sector to be erased.
 The combination of A[20..16] will uniquely select any 64K byte Sector.
2. RD = Data read from location RA during Read operation.
3. PD = Data to be programmed at location PA. Data is latched on the rising edge of WE_L.
4. Read and Byte program functions to non-erasing sectors are allowed in the Erase Suspend Mode.



Command Definitions

The Flash Chip in the device can be read, written and erased. Device erasure and programming are accomplished via the command register within the flash chip. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device.

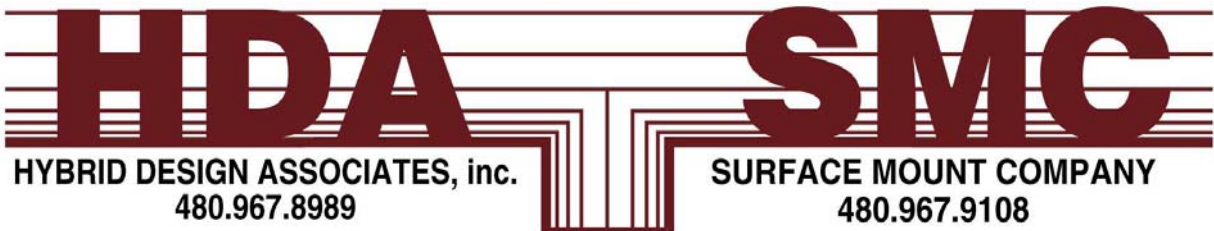
The command register itself does not occupy any addressable memory location. The register is a latch used to store the command along with the address and data information needed to execute the command. The command register is written by bringing WE_L to a low level while CE_L is at a low level and RE_L is high. Addresses are latched on the falling edge of WE_L.

Device operations are selected by writing specific address and data sequences into the command register. Writing incorrect address and data values or writing them in the improper sequence will force the device to the read mode. Table 10 defines the valid register command sequences. Note that the Erase Suspend (BOH) and Erase Resume (30H) commands are valid only while the Sector Erase operation is in progress. Moreover, both Reset/Read commands are functionally equivalent.

Read/Reset Command

The read or reset operation is initiated by writing the read/reset command sequence into the command register. Microprocessor read cycles retrieve array data from the memory. The device remains enabled for reads until the command register contents are altered.

The device will automatically power-up in the read/reset state. In this case, a command sequence is not required to read data. Standard microprocessor read cycles will retrieve array data. This default value ensures that no spurious alteration of the memory content occurs during the power transition.



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Byte Programming

The device is programmed on a byte-by-byte basis within the flash memory chip. Programming is a four bus cycle operation. There are two unlock write cycles. These are followed by the program setup command and data write cycles. Addresses are latched on the falling edge of WE_L and write data is latched on the rising edge of WE_L. The rising edge of WE_L begins programming using an Embedded Program Algorithm. Upon executing the algorithm, the system is not required to provide further controls or timings. The device will automatically provide adequate internally generated program pulses and verify the programmed cell margin.

The automatic programming operation is complete when the data on D07 (also used as Data Polling) is equivalent to the data written to this bit at which time the device returns to the read mode. The device requires that a valid address be supplied at this particular instance of time for Data Polling operations. Data Polling must be performed at the memory location which is being programmed.

Any commands written to the chip during the Embedded Program Algorithm will be ignored. If a hardware reset occurs during the programming operation, the data at that particular location will be corrupted.

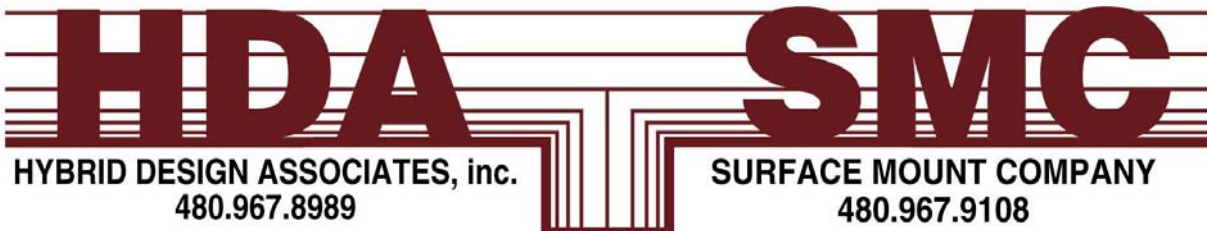
Programming is allowed in any sequence and across sector boundaries. Beware that a data '0' cannot be programmed back to a '1'. Attempting to do so may cause the device to exceed programming time limits or result in an apparent success, according to the data polling algorithm, but a read from reset/read mode will show that the data is still '0'. Only erase operations can convert '0's to '1's.

Chip Erase

Chip erase is a six bus cycle operation. There are two unlock write cycles. These are followed by writing the 'setup' command. Two more 'unlock' write cycles are then followed by the chip erase command.

Chip erase does not require the user to program the device prior to erase. Upon executing the Embedded Erase Algorithm command sequence the device will automatically program and verify the entire memory for an all ones data pattern prior to electrical erase. The erase is performed sequentially one sector at a time. The system is not required to provide any controls or timings during these operations.

The automatic erase begins on the rising edge of the last WE_L pulse in the command sequence and terminates when the data on D07 is '1' (see Write Operation Status section) at which time the device



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returns to read mode.

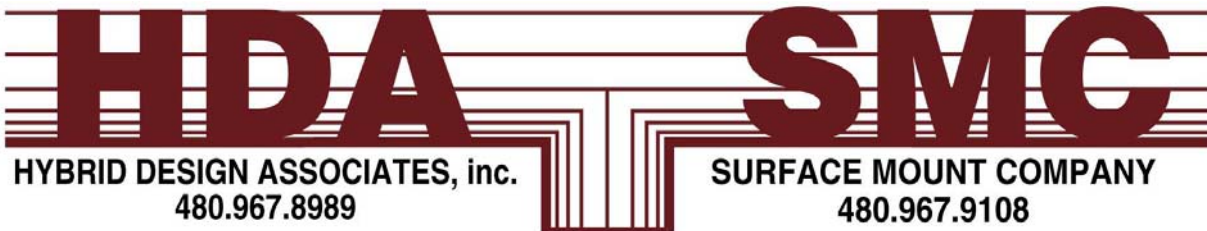
Sector Erase

Sector erase is a six bus cycle operation. There are two 'unlock' write cycles. These are followed by writing the 'setup' command. Two more 'unlock' write cycles are then followed by the sector erase command. The sector address (any address location within the desired sector) is latched on the falling edge of WE_L while the command (30H) is latched on the rising edge WE_L. After a timeout of 50 microseconds the rising edge of the last sector erase command, the sector erase operation will begin.

Multiple sectors may be erased sequentially by writing the six bus cycle operations as described above. This Sequence is followed with writes of the Sector Erase command to addresses in other sectors desired to be sequentially erased. The time between writes must be less than 50 microseconds, otherwise that command will not be accepted and erasure will start. It is recommended that processor interrupts be disabled during this time to guarantee this condition. The interrupts can be reenabled after the last Sector Erase command is written. A timeout of 50 microseconds is from the rising edge of the last WE_L will initiate the execution of the Sector Erase command(s). If another falling edge of the WE_L occurs within the 50 microsecond timeout window the timer is reset (Monitor D03 to determine if the sector erase timer window is still open.) Any command other than Sector Erase or Erase Suspend during this period will reset the device to the read mode, ignoring the previous command string. In that case, restart the erase on those sectors and allow them to complete. Loading the sector erase buffer may be done in any sequence and with any number of sectors (0 to 31) within each of the 16 chips.

Sector erase does not require the user to program the device prior to erase. The device automatically programs all memory locations in the sector(s) to be erased prior to electrical erase. When erasing a sector or sectors the remaining unselected sectors are not affected. The system is not required to provide any controls or timing during these operations.

The automatic sector erase begins after the 50 microsecond time out from the rising edge of the WE_L pulse for the last sector erase command pulse and terminates when the data on D07, Data Polling is correct. At which time the device returns to the read mode. Data Polling must be performed at an address within any of the sectors being erased.



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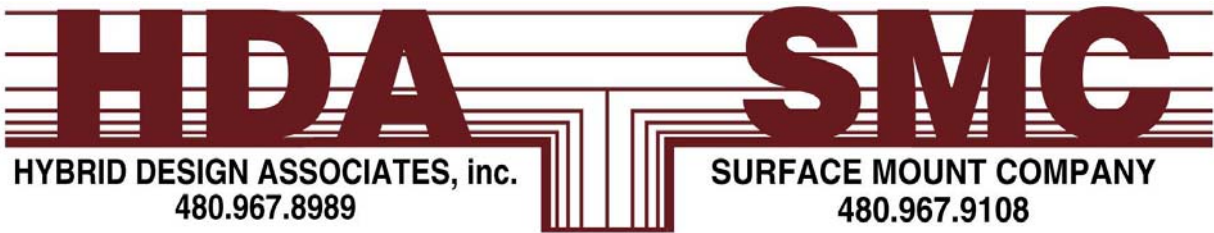
Erase Suspend

The Erase Suspend command allows the user to interrupt a Sector Erase operation and then perform data reads or programs to a sector not being erased. Erase Suspend does not need to be performed if a different flash chip is selected for the read. This command is only applicable for a desired read within the flash chip currently being erased and is also applicable ONLY during the Sector Erase operation which includes the timeout period for sector erase. The Erase Suspend command will be ignored if written during the Chip Erase operation or Embedded Program Algorithm. Writing the Erase Suspend command during the Sector Erase timeout results in immediate termination of the timeout period and suspension of the erase operation.

Any other command written during the Erase Suspend mode will be ignored except the Erase Resume command. Writing the Erase Resume command resumes the erase operation. The addresses are 'don't-cares' when writing the Erase Suspend or Erase Resume command.

When the Erase Suspend command is written during the Sector Erase operation, the device will take a maximum of 15 microseconds to suspend the erase operation. When the device has entered the erase-suspended mode, the FLASHRDY output pin and the D07 bit will be at logic-1, and D06 will stop toggling. The user must use the address of the erasing sector for reading D06 and D07 to determine if the erase operation has been suspended. Further writes of the Erase Suspend command are ignored. When the erase operation has been suspended, the device defaults to the erase-suspend-read mode. Reading data in this mode is the same as reading from the standard read mode except that the data must be read from sectors that have not been erase-suspended. Successively reading from the erase suspended sector while the device is in the erases-suspend-read mode will cause D02 to toggle. After entering the erase-suspend-read mode, the user can program the device by writing the appropriate command sequence for Byte Program. This program mode is known as the erase-suspend-program mode. Again, programming in this mode is the same as programming in the regular Byte Program mode except that the data must be programmed to sectors that are not erase-suspended. Successively reading from the erase-suspended sector while the device is in the erase-suspend-program mode will cause D02 to toggle. The end of the erase-suspended-program operation is detected by the FLASHRDY output pin, Data Polling of D07, or by the Toggle Bit I (D06) which is the same as the regular Byte Program operation. Note that D07 must be read from the byte program address while D06 can be read from any address.

To resume the operation of Sector Erase, the Resume command (30H) should be written. Any further writes of the Resume command at this point will be ignored. Another Erase Suspend command can be written after the chip has resumed erasing.



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Data Polling

DO7

Each Flash chip in the 2MB08F device features Data Polling as a method to indicate to the host that the embedded algorithms are in progress of completion. During the Embedded Program Algorithm, an attempt to read the device will produce the complement of the data last written to DO7. Upon completion of the Embedded Program Algorithm, an attempt to read the device will produce the true data last written to DO7. During the Embedded Erase Algorithm, an attempt to read the device will produce a '0' at the DO7 output. Upon completion of the Embedded Erase Algorithm, an attempt to read the device will produce '1' at the DO7 output.

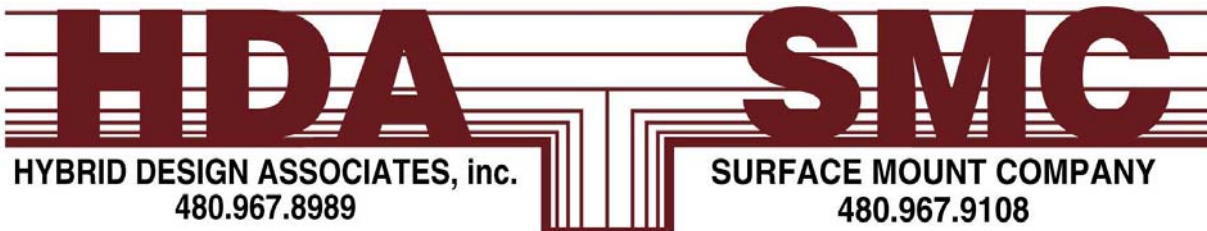
Data Polling will also flag the entry into Erase Suspend. DO7 will switch '0' to '1' at the start of the Erase Suspend mode. Please note that the address of an erasing sector must be applied in order to observe DO7 in the Erase Suspend Mode.

During Program in Erase Suspend, Data Polling will perform the same as in regular program execution outside of the suspend mode.

For chip erase, the Data Polling is valid after the rising edge of the sixth WE_L pulse in the six write pulse sequence. For sector erase, the Data Polling is valid after the last rising edge of the sector erase WE_L pulse. Data Polling must be performed at sector addresses within any of the sectors being erased.

Just prior to the completion of Embedded Algorithm operations DO7 may change asynchronously while the output enable RE_L is asserted low. This means that the device is driving status information on DO7 at one instant of time and then that byte's valid data at the next instant of time. Depending on when the system samples the DO7 output, it may read the status or valid data. Even if the device has completed the Embedded Algorithm operations and DO7 has a valid data, the data outputs on DO0-DO7 may be still invalid. The valid data on DO0-DO7 can be read on the successive read attempts.

The Data Polling feature is only active during the Embedded Programming Algorithm, Embedded Erase Algorithm, Erase Suspend, erase-suspend-program mode, or sector erase timeout.



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Toggle Bit I

DO6

The 2MB08F also features the Toggle Bit I as a method to indicate to the host system that the embedded algorithms are in progress or completed. During an Embedded Program or Erase Algorithm cycle, successive attempts to read (RE_L toggling) data from the device at any address will result in DO6 toggling between '1' and '0'. Once the Embedded Program or Erase Algorithm cycle is completed DO6 will stop toggling and valid data will be read on the next successive attempt. During programming, the Toggle Bit I is valid after the rising edge of the fourth WE_L pulse in the four write pulse sequence. For chip erase, the Toggle Bit I is valid after the rising edge of the Sixth WE_L pulse in the six write pulse sequence. For Sector Erase, the Toggle Bit I is valid after the Last rising edge of the sector erase WE pulse. The Toggle Bit I is active during the sector erase timeout.

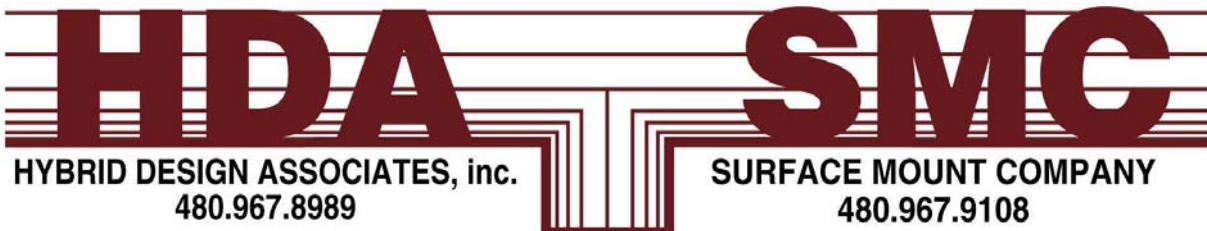
Either CE_L or RE_L toggling will cause DO6 to toggle. Additionally, an Erase Suspend-Resume command will cause DO6 to toggle.

Exceeded Timing Limit

DO5

DO5 will indicate if the program or erase time has exceeded the specified limits (internal pulse count). Under these conditions DO5 will produce a '1' This is a failure condition which indicates that the program or erase cycle was not successfully completed. Data Polling is the only operating function of the device under this condition. The CE_L circuit will partially power down the device under these conditions. The OE_L and RE_L pins will control the output disable functions.

The DO5 failure condition will also appear if a user tries to program a '1' to a location that is previously programmed to '0'. In this case the device locks out and never completes the Embedded Program Algorithm. Hence, the system never reads a valid data on DO7 bit and DO6 never stops toggling. Once the device has exceeded timing limits, the DO5 bit will indicate a '1'. Please note that this is not a device failure condition since the device was incorrectly used. If this occurs reset the device.



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Sector Erase Timer DO3

After the completion of the initial sector erase command sequence the sector erase timeout will begin. DO3 will remain low until the timeout is complete. Data Polling and Toggle Bit I are valid after the initial sector erase command sequence.

If Data Polling or the Toggle Bit I indicates the device has been written with a valid erase command, DO3 may be used to determine if the sector erase timer window is still open. If DO3 is high the internally controlled erase cycle has begun: attempts to write subsequent commands (other than Erase Suspend) to the device will be ignored until the erase operation is completed as indicated by Data Polling or Toggle Bit I. If DO3 is low, the device will accept additional sector erase commands. To insure the command has been accepted, the system software should check the status of DO3 prior to and following each subsequent sector erase command. If DO3 were high on the second status check, the command may not have been accepted.

Toggle BIT II DO2

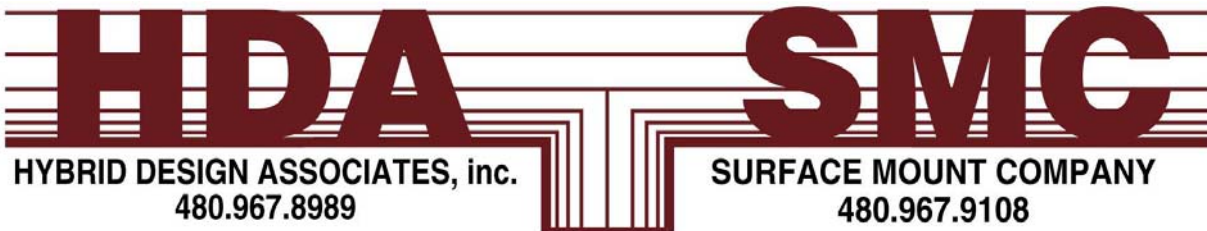
This toggle bit along with DO6, can be used to determine whether the device is in the Embedded Erase Algorithm or in Erase Suspend. Successive reads from the erasing sector will cause DO2 to toggle during the Embedded Erase Algorithm. If the device is in the erase-suspended-read mode, successive reads from the erase-suspend sector will cause DO2 to toggle. When the device is in the erase-suspended-program mode, successive reads from the byte address of the non-erase suspended sector will indicate a logic '1' at the DO2 bit.

DO6 is different from DO2 in that DO6 toggles only when the standard Program or Erase, or Erase Suspend Program operation is in progress.

FLASHRDY_H

This signal on the 2MB08F indicates to the host system that the Embedded Algorithms are either in progress or have been completed. If the output is low, the device is busy with either a program or erase operation. If the output is high, the device is ready to accept any read/write or erase operation. When the FLASHRDY_H pin is low, the device will not accept any additional program or erase commands with the exception of the Erase Suspend command. If the chip is placed in an Erase Suspend mode, the FLASHRDY_H output will be high.

During programming, the FLASHRDY_H pin is driven low after the rising edge of the fourth WE_L pulse. During an erase operation the FLASHRDY_H pin is driven low after the rising edge of the sixth WE_L pulse. The FLASHRDY_H pin will indicate a busy condition during the



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RSTFLASH pulse. This pin should be pulled high by an external pull-up resistor.

RSTFLASH - Hardware Reset

The 2MB08F device may be reset by driving the RSTFLASH pin low. The RSTFLASH pin must be kept low for at least 500 ns. Any operation in progress will be terminated and the internal state machine will be reset to the read mode 20 microseconds after the RSTFLASH pin is driven low. If a hardware reset occurs during a program on erase operation, the data at that particular location will be indeterminate.

When the RSTFLASH pin is low and the internal reset is complete, the device goes to standby mode and cannot be accessed. Also, note that all the data output pins are tri-stated for the duration of the RSTFLASH pulse. Once the RSTFLASH pin is taken high, the device requires 500 ns of wake-up time until outputs are valid for read access.

The RSTFLASH pin may be tied to the system reset input. Therefore, if a system reset occurs during the Embedded Program or Erase Algorithm, the device will be automatically reset to read mode and this will enable the systems microprocessor to read the boot-up firmware from the Flash memory.

Data Protection

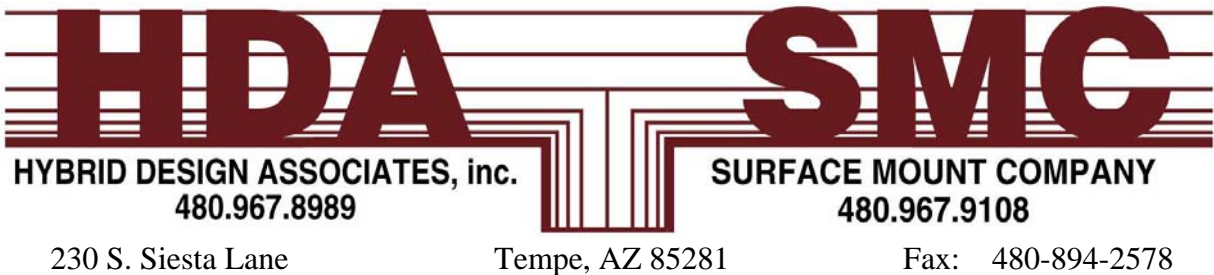
The Flash Chip in the 2MB08F is designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transitions. During power-up, the device automatically resets the internal state machine in the Read mode. Also, with its control register architecture, alteration of the memory contents only occurs after successful completion of specific multi-bus cycle command sequences.

The device also incorporates several features to prevent inadvertent write cycles resulting from VCC power-up and power-down transitions or system noise.

Low VCC Write Inhibit

To avoid initiation of a write cycle during VCC power-up and power-down, Each Flash Chip locks out write cycles for VCC-Vlko (see DC Characteristics section for voltages). When VCC - Vlko, the command register is disabled and all internal program-erase circuits are disabled and the device resets to the read mode. Each flash chip ignores all writes until VCC - Vlko. The user must ensure that the control pins are in the correct logic state when VCC-Vlko to prevent unintentional writes.

Write Pulse “Glitch” Protection



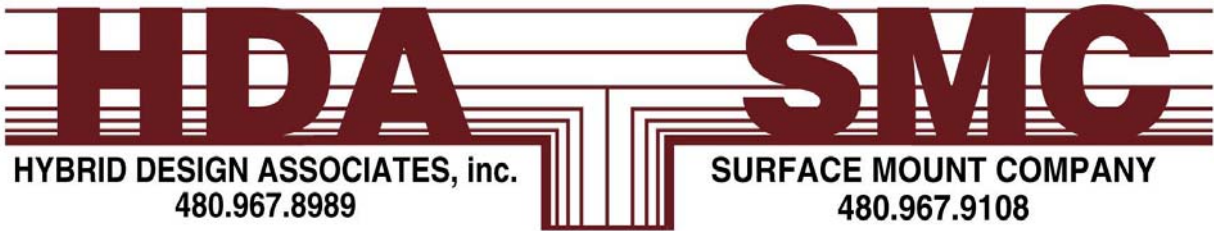
Noise pulses of less than 5ns Typical on RE_L, CE_L or WE_L will not initiate a write cycle.

Logical Inhibit

Writing is inhibited by holding any one of the following signals in the following states:
CE_L = high, WE_L = high, RE_L = Low.

Power-up Write Inhibit

Power-up of the device with WE_L and CE_L in the low state and RE_L in the high state will not accept commands on the rising edge of WE_L. The internal state machines in each flash chip is automatically reset to the read mode on power-up.



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Ordering Information

2MB08F-01 Through Hole 68 PGA Package

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Document Revision History

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1.0	Initial Release	7 September 2006