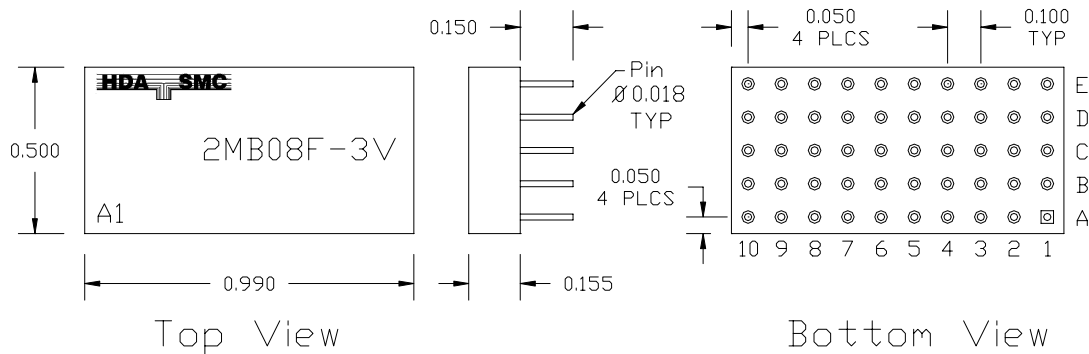


# High Temperature 2MB Flash Memory Module

## Part Number 2MB08F-3V

Preliminary 09/2009  
CMOS 3.0 Volt-only



### CHARACTERISTICS

- DESIGNED FOR HIGH TEMPERATURE APPLICATIONS. DO NOT ERASE ABOVE 100 DEGREES CELSIUS
- 2.7 TO 3.6 VOLT +/- 10% FOR READ AND WRITE OPERATIONS
- SECTOR ERASE ARCHITECTURE
- SUPPORTS FULL CHIP ERASE
- EMBEDDED ERASE ALGORITHMS
- EMBEDDED PROGRAM ALGORITHMS
- DATA POLLING AND TOGGLE BIT FEATURE FOR DETECTION OF PROGRAM OR ERASE CYCLE COMPLETION
- READY/BUSY OUTPUT (FLASHRDY) HARDWARE DETECTION OF PROGRAM OR ERASE CYCLE COMPLETION
- ERASE SUSPEND/RESUME SUPPORTS READING OR PROGRAMMING DATA TO A SECTOR NOT BEING ERASED
- LOW POWER CONSUMPTION
- HARDWARE RESET PIN TO SET INTERNAL STATE MACHINE TO THE READ MODE

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Tempe, AZ 85281

Fax: 480-894-2578

Pin	Description	Pin	Description
A1	D15/A-1	C6	FLASHRDY
A2	BYTE#/WORD	C7	A18
A3	VSS	C8	VCC
A4	A16	C9	WE#
A5	A13	C10	RESET#
A6	A12	D1	D2
A7	VSS	D2	D1
A8	VSS	D3	D0
A9	A15	D4	D11
A10	A14	D5	D10
B1	D13	D6	A17
B2	D14	D7	A7
B3	VSS	D8	D9
B4	D7	D9	A6
B5	D6	D10	A5
B6	A11	E1	VSS
B7	A10	E2	A0
B8	VSS	E3	OE#
B9	A9	E4	D8
B10	A8	E5	A2
C1	D3	E6	A1
C2	D12	E7	A19
C3	VCC	E80	A4
C4	D5	E9	A3
C5	D4	E10	CE#

**Table 1**

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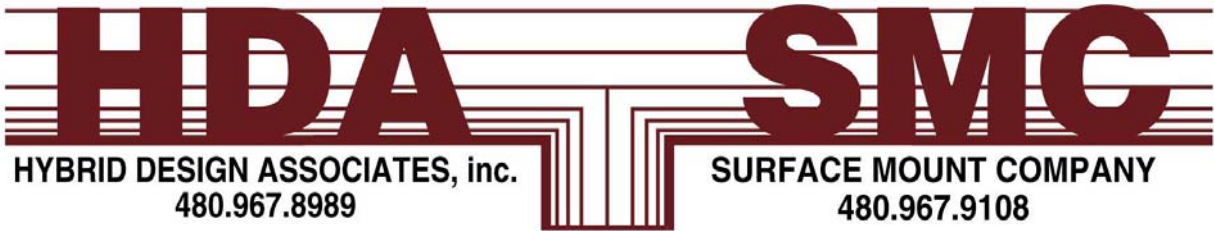
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### Signal Description

VCC + 3 Volts	Power Supply
WE#	Write Enable Asserted Low Input
CE#	Chip Enable Asserted Low Input
RESET#	Reset Flash Asserted Low Input
OE#	Read/Output Enable Asserted Low Input
FLASHRDY	Flash Ready Tristate Output
A[19..0]	Address Inputs
D[14..0]	Data Input/Outputs
D15/A-1	D15 (Data Input/Output, Word Mode) / A-1 (LSB Address Input, Byte Mode)
VSS - GND	Ground

**Table 2**



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## Ordering Information

### **2MB08F-3V Through Hole 50 Pin Grid Array Package**

Hybrid Design Associates, Inc.

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Document

Revision History

Revision No.	Description	Date
1.0	Initial Release	9 February 2009